AN 1715

UHF RFID PCB antenna design

Rev. 3.0 – January 21 2010 Application note

Document information

Info	Content
Keywords	UCODE EPC G2, G2XM, G2XL, Reference Design, Antenna Design, PCB
Abstract	This application note provides basic antenna knowledge, which is important for PCB antenna design. It contains as well a reference design based on a slot antenna.

Revision history

Rev	Date	Description
3.0	20100121	Modify figures and tables of Chapter 6
2.0	20090412	Add Reference Designs (Chapter 6)
1.0	20090311	First initial release; Authors: Barbara Ribic

1. Introduction

Currently an increased interest for the integration of RFID (Radio Frequency Identification) technology in Printed Circuit Boards (PCBs) is observed. The main driver for this development is the possibility of tracking and tracing PCBs during the manufacturing process. However, the spectrum of possible applications for an RFID enabled PCB is broad. It can significantly decrease the inventory time, but could be also used in the end product for a variety of reasons, such as anti counterfeiting of high-valued products or the return handling of goods.

Among all the sub-technologies within RFID, passive UHF RFID seems to be a suitable choice for this application. Depending on the antenna design and the system parameters, read ranges of up to 10 m can be achieved. In most tracking and tracing applications however, a few centimeters will be enough. The read range can therefore be defined in a variable way.

NXP`s latest UHF RFID products (UCODE G2XM, UCODE G2XL) use a standardized air interface protocol (EPC global Class 1 Generation 2), which ensures an effective usage of the available frequency band within the corresponding national regulation.

The main challenge in achieving a good UHF system performance is to combine a sophisticated IC with a suitable label antenna design. IC characteristics such as Q factor and sensitivity, antenna geometry, choice of material and quality of simulation is crucial.

This application note covers initially basic antenna know-how (Chapter 2). It is valid for PCB antenna designs as well as for standard UHF label antenna designs. In both cases the physical boundary conditions need to be taken into account while designing an antenna. Given the basic tools, the special case of a PCB antenna is investigated (Chapter 4).

In chapter 5 we start the practical consideration. As the position of the slot antenna usually cannot be freely chosen due to very little design flexibility regarding the PCB components, different variants of a slot antenna are shown. All findings are based on thorough 3-D simulations.

Chapters 6 and 7 deal with the NXP reference antenna designs for PCB boards. This design was first simulated, then prototyped, and as a final step the simulation results were verified by measurements conducted in an anechoic chamber. It should give our customers a starting point for adapting the design to their own PCB board. In a step-by-

step approach the document will guide the reader starting from antenna design basics through design and simulation to a final antenna solution for PCBs.

2. Antenna basics

This chapter deals with the physical basics behind any UHF label antenna. It should give an impression of which parameters have the main impact on the end performance. These are general considerations, valid for PCB antenna designs as well as for label antenna designs.

2.1 Basic antenna parameters

2.1.1 Input Impedance

The input impedance is the parameter, which describes the antenna input behavior as a circuit element. As usual in electronic circuit design it is important to match this input impedance ($\underline{Z}_{antenna}$) to a given source impedance, which is in case of RFID applications usually the chip impedance of the transponder IC ($\underline{Z}_{chip}$). The maximum power delivered from the source to the antenna is given if the antenna input impedance is complex conjugate to the chip impedance.

Practical: The better the matching, the less power is reflected on the connection between IC bumps and label antenna pads. This will result in a maximum power transfer to the IC. An UHF RFID IC is an ultra low power design, therefore matching is essential in order to make the good sensitivity of the IC result in excellent read ranges in an end application.

2.1.2 Radiation Resistance

The radiation resistance of an antenna is equivalent to a resistance that would dissipate the same amount of power as the antenna radiates, when the current in this resistance is equal to the current at the antenna input terminals.

The total resistance of an antenna ($R_{antenna}$) can be separated into a series circuit of two

$$R_{antenna} = R_{rad} + R_{loss} \quad (1)$$

resistors (equation (1)).

Where R_{rad} is the radiation resistance and R_{loss} is the loss resistance representing the unwanted losses caused by the non-perfect conductors and (substrate) materials.

$$R_{loss} = R_{loss,\,con} + R_{loss,\,sub} \quad (2)$$

Accordingly one can further separate this loss resistance into those two contributions (equation (2)).

2.1.3 Gain and Directivity

The ratio of the radiation intensity in any direction *d* to the intensity averaged over all directions is the directive gain of the antenna in that direction. The directive gain along the direction in which that quantity is maximized is known as the directivity of the antenna. The directivity of the antenna multiplied by the radiation efficiency is the gain of the antenna.

In the direction of maximum radiated power density, we get *G* times more power that we would have obtained from an isotropic antenna.

The gain of an antenna gives its ability to focus the radiated power in a particular direction relative to an isotropic point source and is given by:

$$Gain = 4\pi r^2 \left(\frac{S}{P_{in}} \right) \quad (3)$$

The far field power density S (equation) can be calculated using the equation:

$$S = \frac{Pin \cdot Gain}{4\pi d^2} \quad \left[\frac{W}{m^2} \right] \quad (4)$$

Pin ……Average Power at Antenna [W];

Gain ….Numerical Gain;

d…….Distance from Antenna [m].

More generally the gain is related to the directivity of the antenna by the efficiency of the antenna e

$$G(\theta, \phi) = eD(\theta, \phi) \quad (5)$$

where *D* is given by

$$D(\theta,\phi) = \frac{\text{power radiated in a fixed direction}(\theta,\phi)}{\text{total power radiated by the antenna}} \quad (6)$$

In national UHF frequency regulations, radiated power is defined with different terms in the different countries. The two most common terms are EIRP and ERP.

EIRP (Equivalent Isotropic Radiated Power) – mainly used in the US. Fig 1 shows how a directive antenna is related to an isotropic antenna.

ERP (Effective Radiated Power) – mainly used in Europe. The EIRP is related to the ERP by the following relation:

EIRP = ERP * 1.64

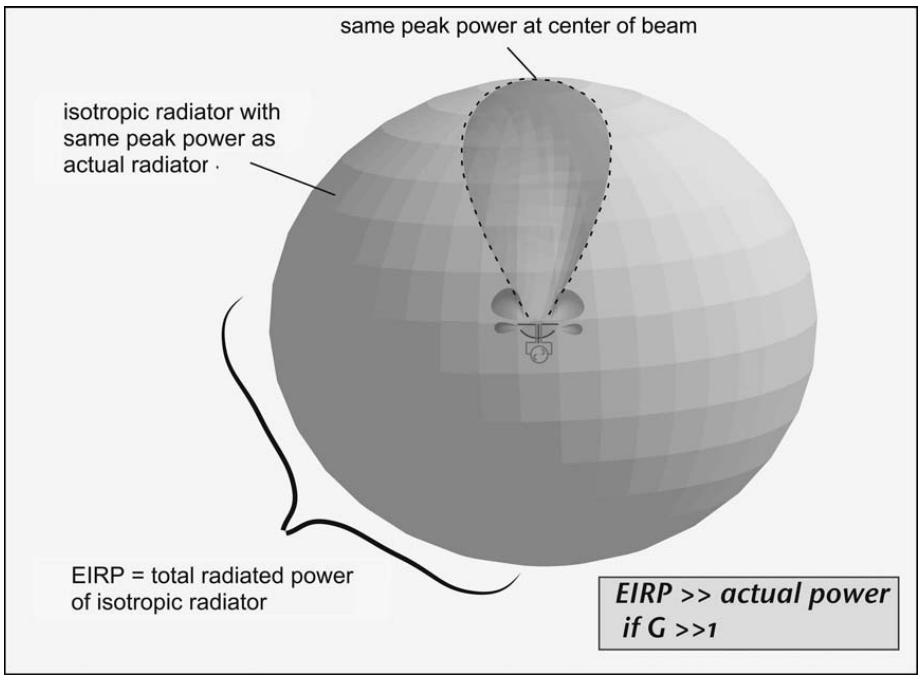


Fig 1. Definition of effective isotropic radiated power

2.1.4 Efficiency

The efficiency of an antenna takes into account the influence of additional losses, which may occur at the input terminals or within the structure of the antenna.

It is the percentage of the power delivered to the antenna that actually gets radiated as opposed to being absorbed or reflected.

For an ideal, lossless antenna, the gain equals the directivity (equation (5)).

Practically, these can be losses due to reflection (mismatching between the IC and the antenna), or conduction and/or dielectric losses.

2.1.5 Bandwidth and Q

The bandwidth can be considered to be the range of frequencies, on either side of a center frequency (for example the resonance frequency of a dipole), where the antenna characteristics (such as input impedance, pattern, beam width, polarization, side lobe level, gain, beam direction, radiation efficiency) are within an acceptable value of those at the center frequency.

An antenna simultaneously stores charge (capacitance), opposes changes in current (inductance), and radiates power into the wide world (resistance). From the electrical point of view, an antenna looks like an R-L-C circuit. The configuration of the circuit depends on the antenna type. A dipole that is short compared to the wavelength looks like a series combination of an inductor and capacitor with some resistance (see Fig 2). The inductance and capacitance are both roughly proportional to the length of the dipole;

In general, the bandwidth is inversely proportional to the Q factor, which is the ratio of the total reactance to the resistance. For a simple series resonant circuit, Q is about twice the voltage amplification factor .Thus, voltage amplification must be traded against bandwidth. Antennas with large reactance (that is, large values of inductance and small values of capacitance) and small values of resistance may be adjusted to be matched to the tag at one frequency, with good power transfer and voltage multiplication, but performance will degrade at other frequencies. Antennas with small reactance will provide better performance over frequency.

$$BW \sim \frac{1}{Q}$$

2.2 Electrical equivalent circuits

For UHF antenna design, it is necessary to investigate the impedances of the system components, meaning, IC, assembly, and tag antenna. The following section describes the impedances from the IC to the tag antenna.

2.2.1 Equivalent circuit of the IC

Electrically, a passive UHF RFID IC can be depicted as a complex, capacitive impedance. Fig 2 shows the equivalent circuit of the input impedance. The impedance value of a UCODE IC is given in the datasheet and also corresponds to the shown serial equivalent circuit.

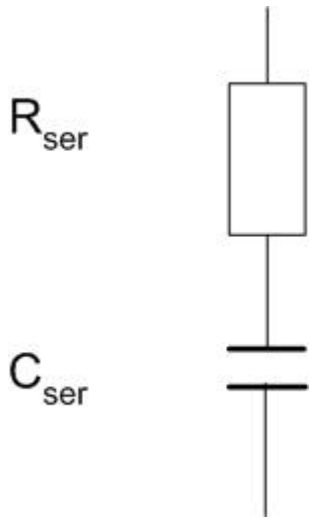


Fig 2. Equivalent circuit of IC input impedance

Note: For the parallel circuit, the values of the real- and imaginary part would change.

2.2.2 Equivalent circuit of the assembled IC

At each assembly process, parasitic capacitances and resistors are inherited, which result in an additional parallel impedance. The value depends on assembly process and parameters.

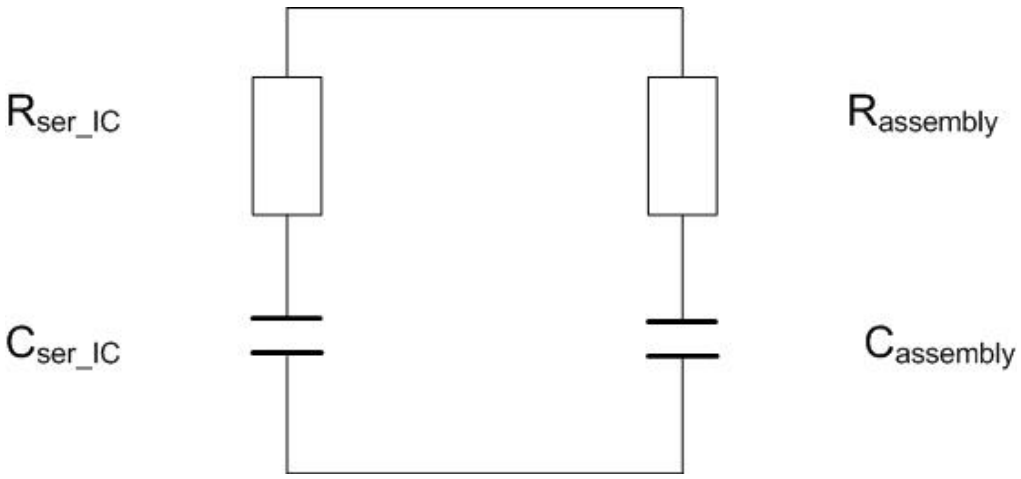


Fig 3. Serial equivalent circuit of assembled IC

2.2.3 Equivalent circuit of a loop antenna

Since the magnetic loop is quite small compared to the wavelength, its near-field components are mainly magnetically. Due to that fact, its reactance is quite insensitive to materials with different electrical permittivity in its close proximity.

The reactance of the magnetic loop can be simply modeled by an inductor. Together with the input capacitance of the IC, an LC-resonating circuit is formed as shown in Fig 4.

The real part of the impedance of the magnetic loop consists of its radiation resistance and an additional resistance representing the losses of the loop antenna. The radiation of a loop-antenna depends on its area relative to the wavelength at the operating frequency. Assuming a loop area of about 2cm² and the wavelength at 915MHz of about 33cm, the radiation resistance can be calculated by following formula (equation (7)) to be:

$$R_{loop,radiation} = 31171 \cdot \frac{A^2}{\lambda^4} = 0.1Ohm \quad (7)$$

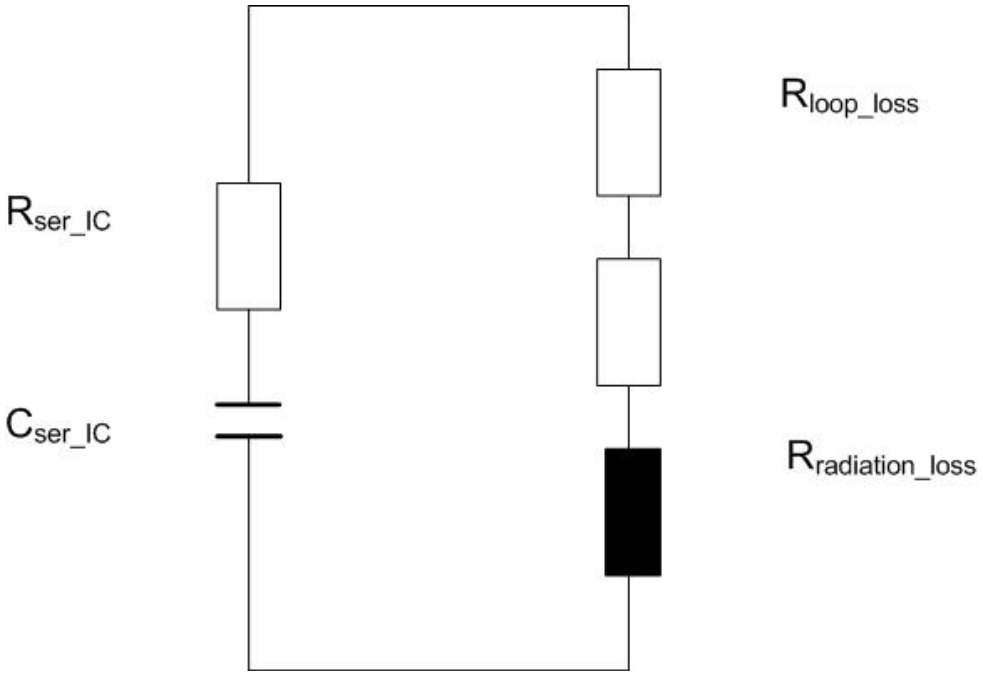


Fig 4. Equivalent circuit magnetic loop

2.2.4 Equivalent circuit of a broadband dipole

A conductor always has a capacitance and an inductance. Hence a dipole in a homogenous electromagnetic field can be represented by a series-L-C resonant circuit.

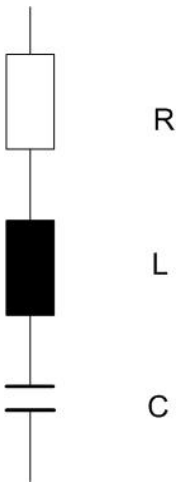


Fig 5. Equivalent circuit of a dipole

The resonance frequency of such a circuit is determined by:

$$\omega_{res} = \frac{1}{\sqrt{LC}} \quad (8)$$

At a given resonance frequency, the product of L and C will result in a certain fixed value. Although the product is fixed the relation of L/C can be chosen arbitrarily. As an example, doubling C and halving L will result in the same resonance frequency. This gives some freedom in the design of the dipole, which means that it is possible to design various kinds of dipoles with different shapes, which all have the same resonance frequency.

The difference between 2 dipoles with the same resonance frequency but a different L/C-ratio is the quality and hence the bandwidth, since

$$Q \sim \sqrt{\frac{L}{C}} \quad (9)$$

And

$$BW \sim \frac{1}{Q} \quad (10)$$

Therefore the L/C-ratio has to be minimized in order to obtain a high bandwidth of the dipole. As an example increasing the thickness of a dipole can achieve this. The increased thickness reduces the self-inductance and the increased surface of the dipole results in an increased capacitance of the dipole. Chapter 4.3 gives further insight on this matter.

2.3 Matching

The input impedance is the parameter, describing the antenna input behavior as a circuit element. As usual in electronic circuit design it is important to match this input impedance ($\underline{Z}_{antenna}$) to a given source impedance, which is in case of RFID applications the chip impedance of the transponder IC ($\underline{Z}_{chip}$). The maximum power delivered from the source to the antenna is given if the antenna input impedance is complex conjugate to the chip impedance:

$$\underline{Z}_{antenna} = \underline{Z}^{*}_{chip} \tag{11}$$

Separated into real- and imaginary parts we get the following conditions:

$$R_{antenna} = R_{chip} \tag{12}$$

$$X_{antenna} = -X_{chip} \tag{13}$$

For designing an efficient antenna it is necessary to match the real part and the conjugate imaginary part of the source impedance (practically this takes into account the IC impedance AND the parasitic assembly impedance). Assuming complex conjugate impedance matching between antenna and chip (assembled) and further assuming the case of a receiving antenna the maximum power delivered from the antenna ($P_{antenna,\,max}$) is:

$$P_{antenna,\,\max} = \frac{\left|\underline{V}_{antenna}\right|^2}{4\,R_{antenna}} \tag{14}$$

Where $V_{antenna}$ is the voltage generated by the label antenna due to receiving an electro-magnetic wave and $R_{antenna}$ is the resistance of the label antenna.

In order to estimate the variation of the read range of a given transponder if the loss impedance is being modified (caused by modifications of the flip chip mounting parameters) the following approach can be followed:

The received (tag) power at an arbitrary point is:

$$P_{Tag} = A_{Tag} \cdot S \quad (15)$$

with: A_{Tag} = Effective Area of the (tag) antenna (derived from radar technique) and S=power density.

Further it is:

$$A_{Tag} = \frac{\lambda_0^2}{4\pi} \cdot G_{Tag} \quad (16)$$

with: λ_0 = wave length ($\lambda_0 = c/f_0$) and
G_{Tag} = gain of tag antenna

And

$$S = \frac{P_{\mathrm{Re}\,ader} \cdot G_{\mathrm{Re}\,ader}}{4\pi \cdot D^2} \quad (17)$$

with: P_{reader}= reader/scanner power,
G_{reader} = gain of reader antenna and
D = maximum distance between tag and reader.

Using Equation (17) and Equation (16) in Equation (15) and solving for the distance D yields:

$$D = \frac{\lambda_0}{4\pi} \cdot \sqrt{\frac{P_{\mathrm{Re}\,ader}}{P_{Tag}} \cdot G_{\mathrm{Re}\,ader} G_{Tag}} \quad (18)$$

Assuming the following data applicable for UHF labels:

λ_0 = 32.8 cm (f_0= 915 MHz),
P_{Reader} = 30 dBm (= 1 W),
G_{Reader} = 2.15 dBi (= 1,642, 100% efficient dipole)
P_{Tag} = -15.23 dBm (= 30 μW, minimum operating power of tag),
G_{Tag} = 2.15 dBi (= 1,642, 100% efficient dipole)

The maximum theoretical distance between transponder and reader can be calculated to be:

D_0 = 7.811 m.

No we can calculate the new distance (which is reduced since energy is short circuited by the loss impedance parallel to the chip) in relation to the maximum theoretical distance. Defining the relative change of the distance yields:

$$\Delta D = \frac{D - D_0}{D_0} \tag{19}$$

Using Equation (18) with P_{Tag} = P0 and P_{Tag}= P respectively yields:

$$\Delta D = \sqrt{\frac{P_0}{P}} - 1 \tag{20}$$

Further the total power received by the tag consists of three terms:

$$P_{Tot} = P_{Chip} + P_{loss} + P_{antenna} \tag{21}$$

The related efficiency for the IC will result in:

$$\eta_{Chip} = \frac{P_{Chip}}{P_{tot}} = \frac{P_{Chip}}{P_{Chip} + P_{loss} + P_{antenna}} \tag{22}$$

Regarding the total received tag power (P_{tot}) we have to differ two cases:

1.) Ideal case

Theoretical maximum distance with no losses and optimum impedance matching between antenna and chip, which yields:

$$P_0 = P_{tot} = P_{Chip} + P_{loss} + P_{antenna} \tag{23}$$

With P_{loss} = 0 (no losses) and P_{chip} = $P_{antenna}$ (power matching) we get:

$$P_0 = 2 \cdot P_{Chip} \quad (24)$$

2.) Real case

Taking into consideration the parallel loss impedance, which yields:

$$P = P_{tot} = \frac{P_{Chip}}{\eta_{Chip}} \quad (25)$$

Using equation (22) and equation (23) in equation (20) yields the change in the distance between label and reader in relation to the theoretical maximum range:

$$\Delta D = \sqrt{2 \cdot \eta_{Chip}} - 1 \quad (26)$$

The matching system is shown by a simplified equivalent network consisting of the chip, the loss impedance, and the antenna (including an ideal voltage source). Fig 6 shows the related network. The elements of the transponder are substituted by series circuits of resistors and capacitors (chip and loss impedance) and a resistor and an inductance (antenna). All elements are parallel connected. The voltage source V_Antenna represents the voltage of the antenna generated by the received electromagnetic wave.

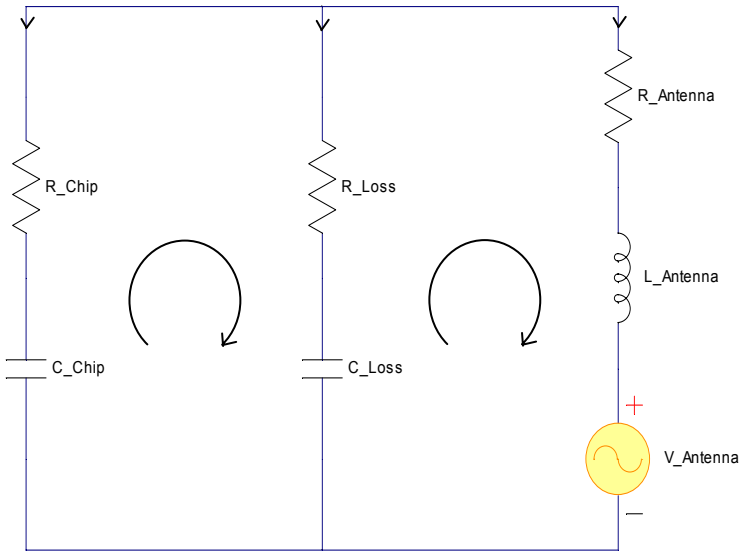


Fig 6. Equivalent electrical circuit of a transponder

2.4 Reflection coefficient

Especially at high frequencies such as e.g. UHF the mismatch between a source and a load (or in general between to elements) is represented by the reflection coefficient $\underline{\Gamma}$. Based on transmission line theory this reflection coefficient is defined by the ratio of the reflected wave to an incident wave. Hence the reflection coefficient is simply a measure of the quality of the match between the source- and the load impedance. Therefore the dimensionless complex reflection coefficient is defined by:

$$\underline{\Gamma} = \frac{\underline{Z} - \underline{Z}_0^*}{\underline{Z} + \underline{Z}_0} \quad (27)$$

Where $\underline{Z}$ is the measured impedance and
$\underline{Z}_0$ is the normalizing impedance

Very often the imaginary part of $\underline{Z}_0$ is zero (or can be neglected) and the real part is fixed

$$\underline{\Gamma} = \frac{\underline{Z} - R_0}{\underline{Z} + R_0} \tag{28}$$

to R_0 = 50 Ω, which results in a reflection coefficient of:

Further more the reflection coefficient is usually given as a logarithmic data (in dB):

$$\Gamma_{dB} = 20 \cdot \lg\left(\left|\underline{\Gamma}\right|\right) \tag{29}$$

The above equation has to be used for amplitudes like e.g. voltages. Whereas the factor 20 has to be replaced by the factor 10 if powers i.e. square of amplitudes are considered.

Another derivation of the reflection at a port of a device is based on the network analysis theory of a two-port device (or network) and it's related scattering parameters. Two-port s-parameters are defined by considering a set of voltage waves. Those voltage waves are being divided by the square root of reference impedance. If further the square of the magnitude of these new variables is being considered one gets traveling power waves:

$|\underline{a}_1|^2$ = incident power wave at the network input

$|\underline{b}_1|^2$ = reflected power wave at the network input

$|\underline{a}_2|^2$ = incident power wave at the network output

$|\underline{b}_2|^2$ = reflected power wave at the network output

These variables are related in the following equation system:

$$\begin{aligned} \underline{\boldsymbol{b}}_1 &= \underline{\boldsymbol{a}}_1 \cdot \underline{\boldsymbol{s}}_{11} + \underline{\boldsymbol{a}}_2 \cdot \underline{\boldsymbol{s}}_{12} \\ \underline{\boldsymbol{b}}_2 &= \underline{\boldsymbol{a}}_1 \cdot \underline{\boldsymbol{s}}_{21} + \underline{\boldsymbol{a}}_2 \cdot \underline{\boldsymbol{s}}_{22} \end{aligned} \tag{30}$$

A two-port network with its related power waves is presented in Fig 7.

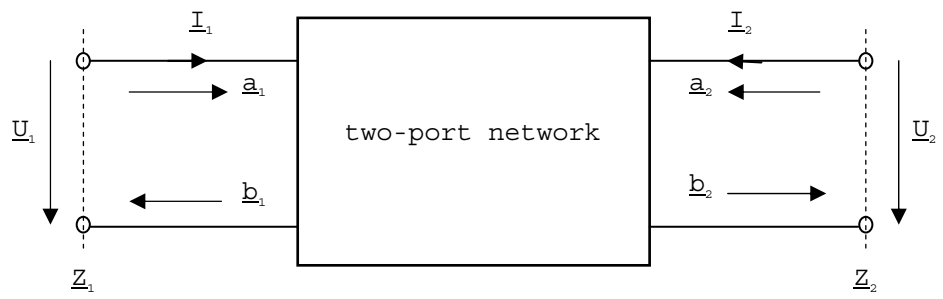


Fig 7. Two-port network with wave-parameter

Terminating the output of a two-port device with the reference impedance causes no reflection at the output and hence $\underline{a}_2$ is zero, then we get:

$$\underline{s}_{11} = \left.\frac{\underline{b}_1}{\underline{a}_1}\right|_{a_2=0} \equiv \text{input reflection coefficient}$$
$$\underline{s}_{21} = \left.\frac{\underline{b}_2}{\underline{a}_1}\right|_{a_2=0} \equiv \text{forward transmission coefficient} \quad (31)$$

Driving the two-port device (or network) from the output terminal and terminating the input port with the reference impedance causes no reflection at the input and hence $\underline{a}_1$ is zero, then we get:

$$\underline{s}_{22} = \left.\frac{\underline{b}_2}{\underline{a}_2}\right|_{a_1=0} \equiv \text{output reflection coefficient}$$
$$\underline{s}_{12} = \left.\frac{\underline{b}_1}{\underline{a}_2}\right|_{a_1=0} \equiv \text{reverse transmission coefficient} \quad (32)$$

Per definition the scattering parameter $\underline{s}_{11}$ is equal to the reflection coefficient $\underline{\Gamma}$ as described above. Usually the scattering parameters are also given in decibel (dB).

The traditional way to determine the reflection coefficient ρ is to measure the standing wave caused by the superposition of the incident wave and the reflected wave. The ratio of the maximum divided by the minimum is the Voltage Standing Wave Ratio (VSWR). The VSWR is infinite for total reflections because the minimum voltage is zero. If no reflection occurs the VSWR is 1.0. VSWR and reflection coefficient are related as follows:

$$VSWR = \frac{(1+|\rho|)}{(1-|\rho|)} \quad (33)$$

Most present instrumentation measures the reflection coefficient and calculates the VSWR.

2.5 Label Antenna Design

The antenna design is one of the most critical point in passive UHF RFID systems. As described in the previous sections the antenna transfers the radiated power from the reader antenna to the IC. In order to achieve the maximum power transfer, the antenna impedance (Z_{Ant}) must be the complex conjugate of the IC impedance (Z_{IC}):

$$Z_{Ant} = Z_{IC}^{*} \tag{34}$$

The antenna is directly connected to the chip, which typically presents a high-capacitive input impedance. The mechanical process of direct attaching the IC to the antenna introduces further parasitic capacitance between the IC and the antenna. The parasitic capacity due to the assembling process is considered in parallel to the IC, therefore they are added to the IC capacitance (in case of equivalent parallel model of the IC).

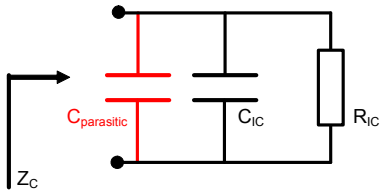


Fig 8. Equivalent circuit of the IC including parasitic.

By taking into account the parasitic effects of the mechanical assembly process, the new impedance of the assembled IC (calculated and or measured) is denoted as Z_C .

To achieve the best matching between the antenna and the IC the following equation must be satisfied.

$$Z_{Ant} = Z_{C}^{*} \tag{35}$$

Of course due to physical restriction the exact matching most of time in real life application can not be achieved.

A way to obtain the best matching between the antenna and the IC is to minimize the power reflection coefficient $|s|^2$ in the following equation:

$$|s|^2 = \left| \frac{Z_{Ant} - Z_C^*}{Z_{Ant} + Z_C} \right|^2 \quad (36)$$

By knowing the tag antenna parameter, it is possible to calculate the RFID tag performance by following:

$$Range = \frac{\lambda}{4\pi} \sqrt{\frac{P_{eirp} G_r}{P_{th}} p\left(1 - |s|^2\right)} \quad (37)$$

Where λ is the wavelength, P_{eirp} is the equivalent isotropic radiated power transmitted by the reader, G^r is the tag antenna gain, P_{th} is the minimum power required to activate the chip (as provided in the datasheet), and p is the polarization loss factor.

3. Packages

In RFID, usually a bare die is directly assembled to a label. For PCBs however, packaged RFID chips are preferred as they are easier to handle and withstand reflow soldering and physical stress.

This chapter contains an overview of the available packages of the NXP UCODE G2XM IC, which are suitable for the application of PCB tagging.

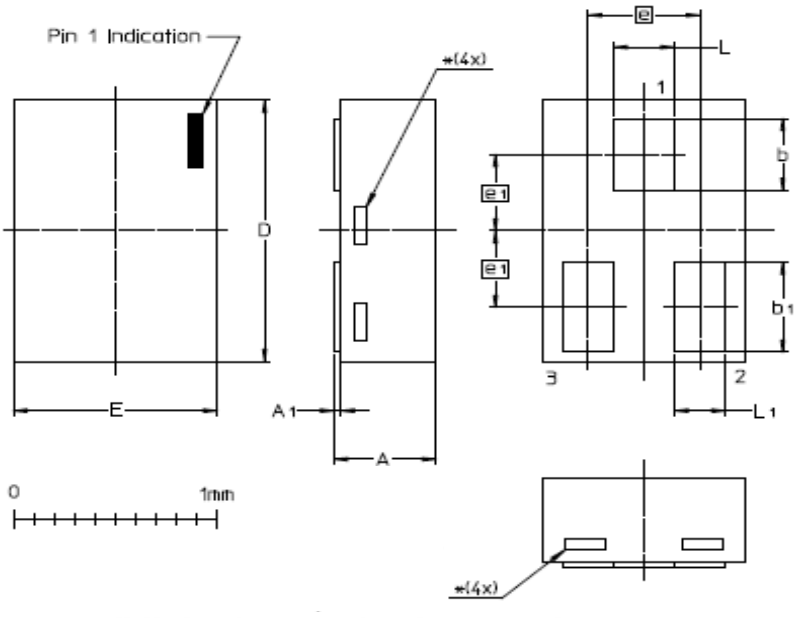
Details on the package can be found in the functional specification of the UCODE G2XM and the UCODE G2XL IC.

3.1 SOT1122 package

Below information is based on engineering material. The SOT1122 parts will be orderable from cw 23 2009 onwards, including the final datasheet and final impedance values.

Impedance parameters of SOT1122:

Symbol	Parameter	Typ	Unit
C_{in}	Input capacitance	1010	pF
Z_{915}	Impedance (915 MHz)	19 - j172	Ohm



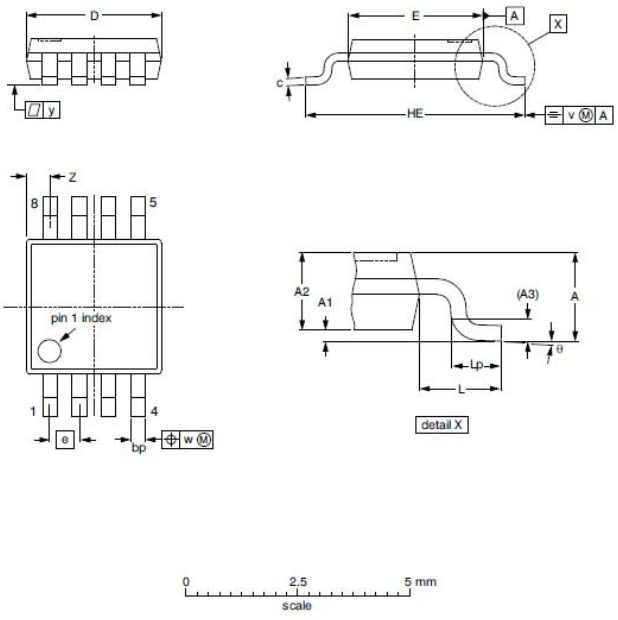
UNIT	A	A_1	D	E	e1	e	b	b_1	L	L_1
min			1.40	0.95			0.37	0.47	0.27	0.22
nom			1.45	1.00	0.425	0.55	0.40	0.50	0.30	0.25
max	0.50	0.04	1.50	1.05			0.45	0.55	0.35	0.30

Fig 9. Package Specification of the UCODE G2XM SOT1122

3.2 TSSOP8 package

Impedance parameters of TSSOP8:

Symbol	Parameter	Typ	Unit
C_{in}	Input capacitance	1160	pF
Z_{915}	Impedance (915 MHz)	16-j148	Ohm



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A1	A2	A3	bp	c	D(1)	E(2)	e	HE	L	Lp	v	w	y	Z(1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.1 2.9	3.1 2.9	0.65	5.1 4.7	0.94	0.7 0.4	0.1	0.1	0.1	0.70 0.35	6° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-1						~~99-04-09~~ 03-02-18

Fig 10. Package Specification of the UCODE G2XM TSSOP8

4. PCB

If an antenna should be integrated on a Printed Circuit Board (PCB) the same UHF principles as explained in Chapter 2 apply. The boundary conditions however are different from the standard label antenna design.

The dielectric parameters of the substrate material are crucial for the correct matching and design of a PCB antenna:

The dielectric plays especially in the UHF RFID frequency range an important role, as the information transmission mainly takes place over the far field, where the electrical component (opposed to the magnetic component) is predominating.

The electrical flux density D is depending on the electric field E and the permittivity of the media ε. The permittivity can be considered as a scalar or a tensor, the D and the E field are parallel, see equation (0 below).

$$D = \varepsilon E = \varepsilon_0 \varepsilon_R E \quad (38)$$

ε_0 denotes the vacuum permittivity and ε_R the dielectric constant of the transmission media.

A label antenna applied on a carrier material of a high dielectric constant, has to be able to handle two effects, in order to keep a good performance:

Detuning: Detuning of the label resonance frequency will lead to mismatch and to performance loss. It needs a dedicated antenna design for high dielectric carriers.

Attenuation: Depending on the imaginary part of the dielectric constant of the media (carrier material), a certain amount of UHF waved will be absorbed and reduce as well the read range.

4.1 What parameters should be taken into account when designing an UHF antenna for a PCB?

A solid design is based on simulations. Therefore, certain boundary conditions are given upfront:

Substrate Material: The permittivity value of the substrate material needs to be taken into account during the simulation, in order to achieve a good matching between antenna and (packaged) IC. In most cases, the PCB material is FR4, having an ε_R of 4.4.

Layers: In most cases the PCB will have 4 layers, which have internal interconnections. The copper antenna will be placed on one of the outer layers (top or bottom).

Thickness: Thickness of substrate material as well as thickness of metal (copper) antenna influences the performance.

Dimension: Size of the PCB, dimensions of the antenna, width and length of the slot.

Geometry: Placement of the antenna an the board.

IC attachment: Packaging of the IC and assembly will influence the impedance (parasitic capacitances).

5. Theory Slot Antenna

The classical UHF label design is a loop in combination with a dipole, as it is also described in the theoretical part of this document (Antenna basics).

For the PCB application, the critical parameter is the space on the PCB. After thorough investigations, the slot antenna concept was chosen to be the most suitable approach. It is an elaborated trade-off between minimum space requirement, and maximum read range.

This chapter gives first an introduction on the theory of slot antennas. The main emphasis however was put on practical questions, such as dimensioning of the slot, and its placement on the PCB. The investigations regarding the placement are based on simulations.

Practical design examples are provided in Chapter6. Chapter 6.3 also describes a practical approach to a loop antenna design.

5.1 Slot Antenna Basics

The antenna type which was used for the NXP PCB reference design is a slot antenna. Due to the fact that it consumes a minimum of space, and has a maximum performance (compared to a simple loop antenna) this approach was chosen.

The basic slotline consists of a dielectric substrate with a narrow slot etched in the metallization on one side of the substrate (Fig 11). The other side of the substrate is without any metallization (FR4, in our case).

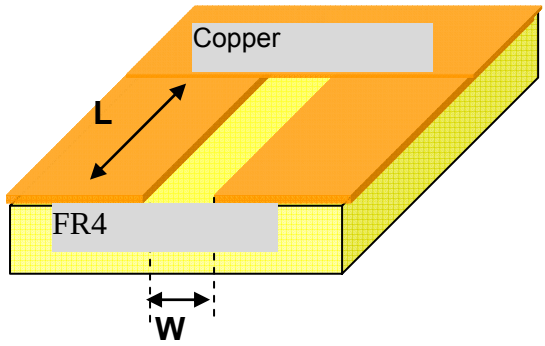


Fig 11. Slotline antenna on a PCB

In a slotline, the wave propagates along the slot with the major electric field component oriented across the slot in the plane of metallization on dielectric substrate.

The slot has a certain length “L” and a width “W”.

5.2 Slot Dimension

Below section shows how the slot dimensions should be, in order to match the packaged IC impedance. It is crucial to have a good matching, in order to ensure an efficient power transfer from the antenna to the IC as well as from the IC to the antenna.

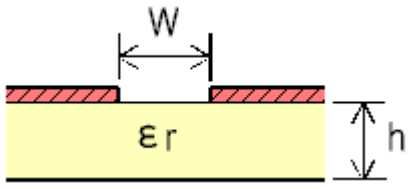


Fig 12. Parameters for the slot definition

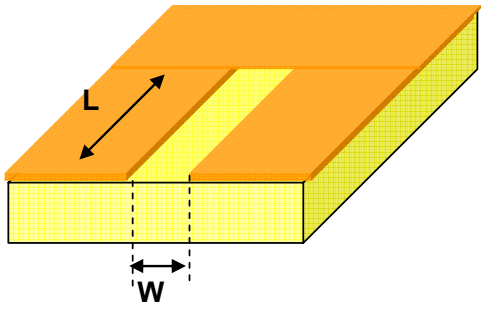


Fig 13. Outline of slot parameters

A slot line can be seen as a transmission line.

In the PCB antenna case in particular it can be seen as a slot line closed on a load (short circuit).

The equivalent circuit of the packaged IC connected to the PCB antenna is depicted in Fig 14. The IC equivalent is shown as the voltage source "V_g" and the impedance "Z_g" (capacitive). The inductive impedance value of the slot antenna is given by "Zin", while Z_{in} is depending on Z_L (load impedance) andZ_0.(Impedance depending on the length of the conductor).

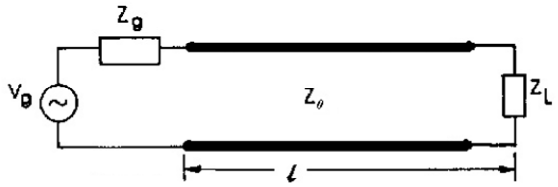


Fig 14. Electrical Equivalent circuit (IC and antenna)

In order to have the maximum power transfer from the "source" (RFID IC) to the "load" (transmission line with length ***L,*** characteristic impedance ***Z_0***, and terminated on load Z_L), following condition shall be fulfilled:

$$Z_{IC} = Z_{IN}^*$$

The transmission line input impedance must be the complex conjugate if the packaged IC impedance.

$$Z_{IN} = Z_0 \frac{\left[Z_L \cos(\beta L) + jZ_0 \sin(\beta L)\right]}{\left[Z_0 \cos(\beta L) + jZ_L \sin(\beta L)\right]} \quad (39)$$

The input impedance of the transmission line can be calculated from:

Where Z_0 solved in non closed form for 0.2<W/h<1

Is given by [1]:

(40)

$$Z_0 = 113.19 - 53.55\log(\varepsilon_{reff}) + 1.25(W/h)(114.59 - 51.88\log(\varepsilon_{reff})) +$$
$$+ 20(W/h - 0.2)(1 - (W/h)) -$$
$$(0.15 + 0.23\log(\varepsilon_{reff}) + (W/h)(-0.79 + 2.07\log(\varepsilon_{reff})))$$
$$(10.25 - 5\log(\varepsilon_{reff}) + (W/h)((2.1 - 1.42\log(\varepsilon_{reff}))) - (h/\lambda_0)100)^2$$

The field components are not confined to the substrate alone. They extent into the air regions above the slot and also below the substrate. Therefore, the energy is distributed between the substrate and the air regions. Consequently, the effective dielectric constant for a slotline (ε_{reff}) is less than the substrate permittivity ε_r.

The effective dielectric constant can be calculated with following formula:

$$\varepsilon_{reff} = \frac{(\varepsilon_r + 1)}{2} + 1 \quad (41)$$

The free space wavelength λ_0 is defined by below equation:

$$\lambda_0 = \frac{v}{f} \quad (42)$$

,whereby:

v = speed of light (3*10^8)

f = 915 MHz

Where β denotes the propagation constant (ideal system, no losses).

(43)

$$\beta = (2\pi/\lambda_0)\sqrt{\left(1/\lambda_s/\lambda_0\right)^2 - 1}$$

λ_s denotes the slot wavelength.

Due to the complexity of calculating such a system, closed-form expressions are used. Depending on the ratio between width (W) and height (h) as shown in Fig 12, following formula can be used as an approximation [1]:

For 0.2<= W/h<= 1.0 :

$$\frac{\lambda_s}{\lambda_0} = 0.987 - 0.483\log(\varepsilon_{reff}) + \\ + W/h(0.111 - 0.0022\varepsilon_{reff}) - \\ - (0.121 + 0.094(W/h) - 0.0032\varepsilon_{reff})\log(100(h/\lambda_0)) \quad (44)$$

Practical example (1):

IC:

To match assembled IC with an equivalent series impedance of

Z_{IC} = 20-j140

PCB:

Assuming a PCB with following properties:

Carrier material (substrate): FR4 (ε_R = 4.4)

Substrate height h = 1.5mm

Slot line:

Definitions of the slot dimensions:

Width W = 0,6 mm

Length L = 37,1 mm

Matching:

Setting the parameters in equations (39) till (44) leads to input impedance on the line (assumption: no losses) of:

Z_{in} = 0 + j140,41

This gives a best matching of the imaginary part of the complex impedance.

Note:

Equations (40) and (44) are approximations, and give an indication of the geometrical parameters.

5.3 Slot Placement

Following chapter shows the influence of the placement of the slot. 5 different cases are evaluated. The ideal case is a symmetrical placement. However, often this is not possible due to certain boundary conditions regarding the layout of the PCB.

The positioning influences the antenna impedance, which is shown by smith charts.

The impedance of the antennas is inductive, and therefore the impedances are located in the upper hemisphere of the Smith chart.

For the simulations, following boundary conditions were chosen:

IC attachment: Direct, without package

Assembled IC: capacity: 1,3 pF

Antenna material: copper

PCB material: FR4, ideal ε_R = 4.4

Changing the position of the slot means changing the antenna impedance, but most of all changing the antenna gain. The radiation characteristic of an antenna is mainly determined by the antenna geometry. An asymmetric geometry will influence the current (field) distribution.

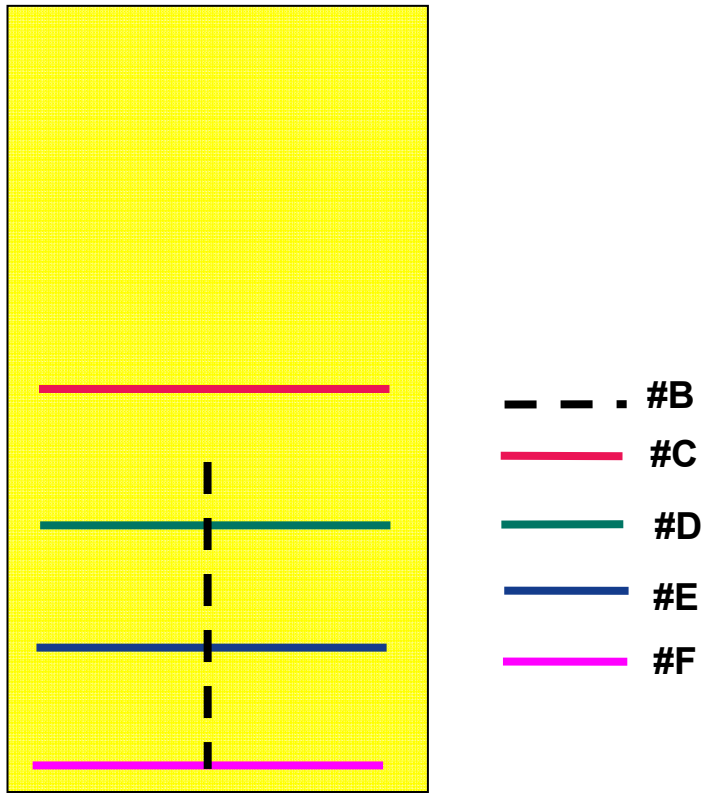


Fig 15. Simulated slot positions B-F

5.3.1 Position B

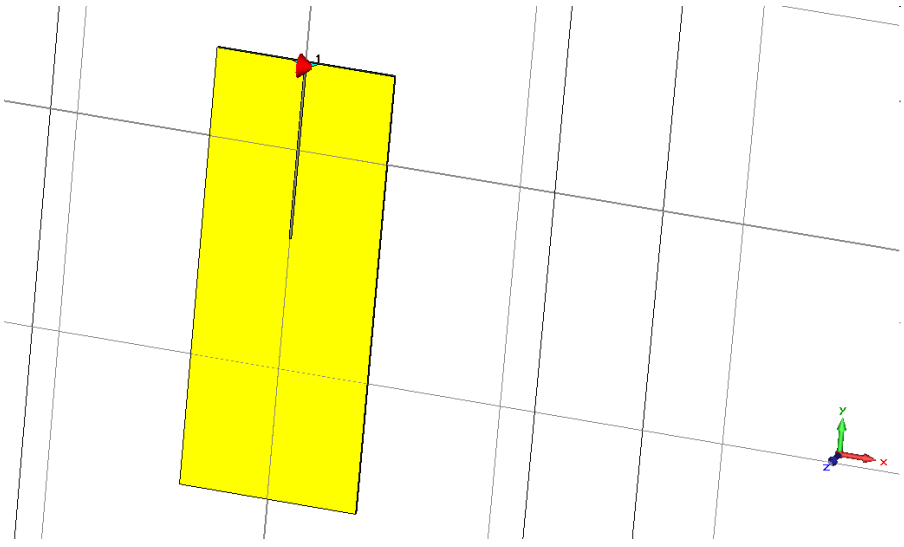


Fig 16. Slot positioning- Case B

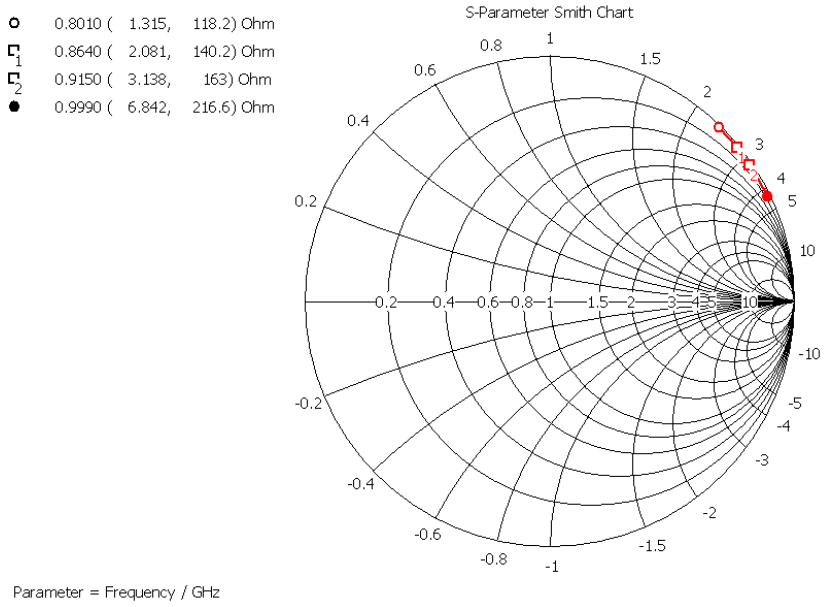


Fig 17. Smith Chart Position B : Simulated impedance of the PCB antenna for 4 different frequencies

Fig 17 shows the simulated impedance of the antenna in a frequency range between 801 MHz and 999 MHz. At 915 MHz, the impedance is 3,1 +j163 Ω.

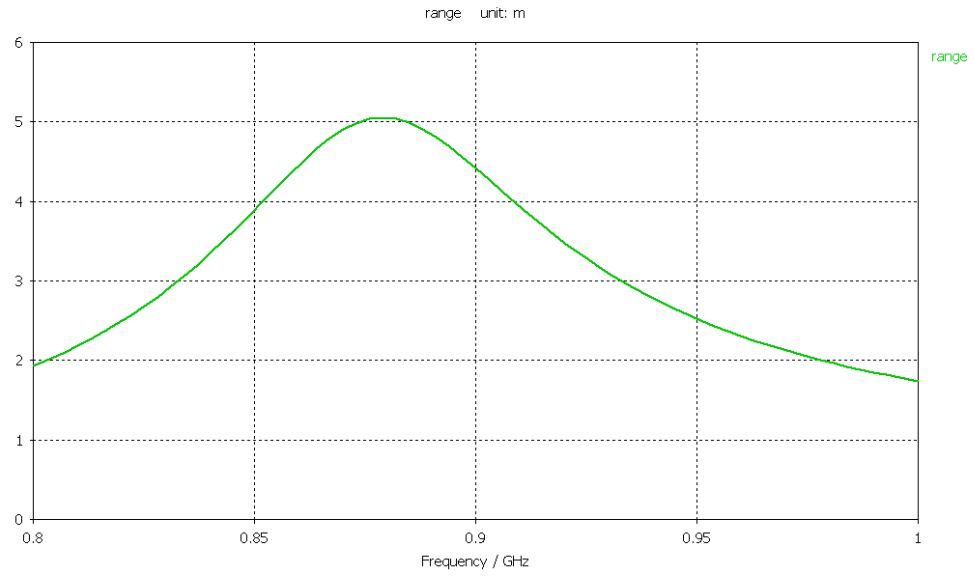


Fig 18. Simulated read range for slot position B

Fig 18 shows the simulated read range over a frequency band from 800 MHz to 1 GHz. The resonance point is located at approximately 875 MHz.

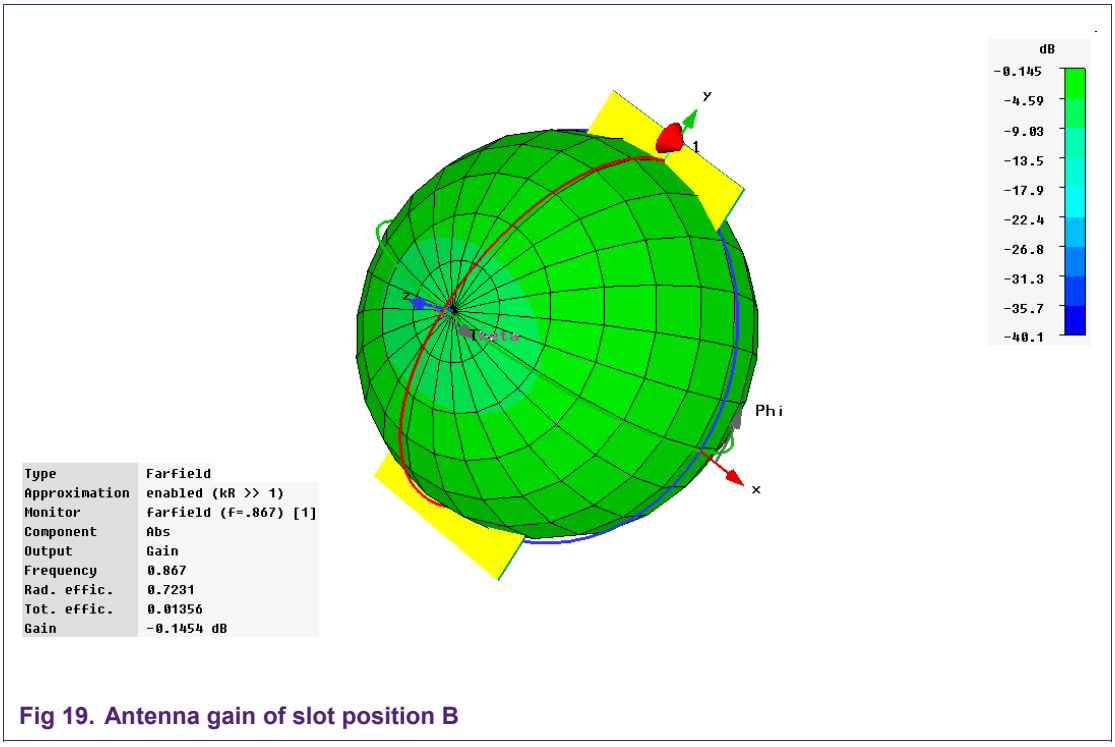


Fig 19. Antenna gain of slot position B

Fig 19 shows the total gain of the position B antenna. The maximum gain has a negative value of – 0,145 dBm.

5.3.2 Position C

Position C is symmetrically placed at the middle of the long side of the PCB.

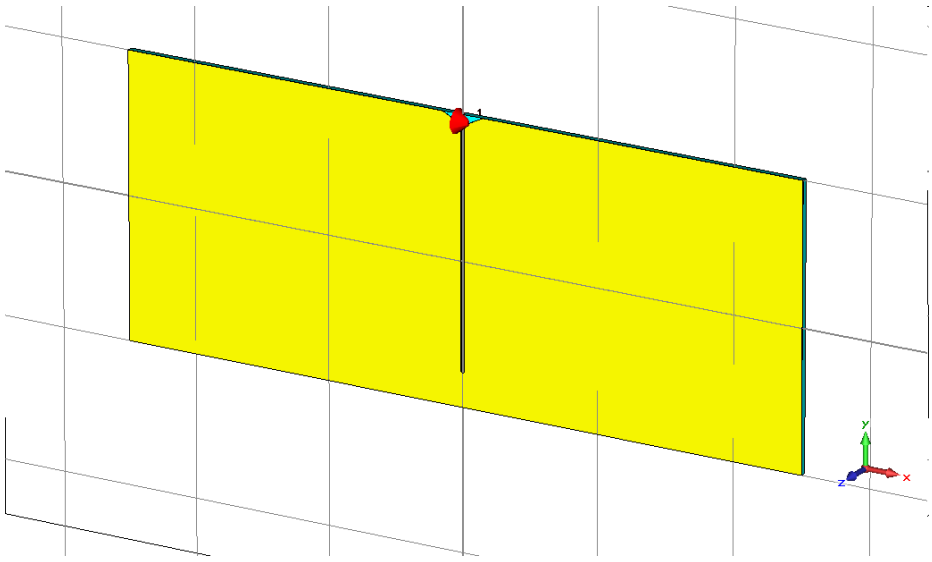


Fig 20. Slot positioning- Case C

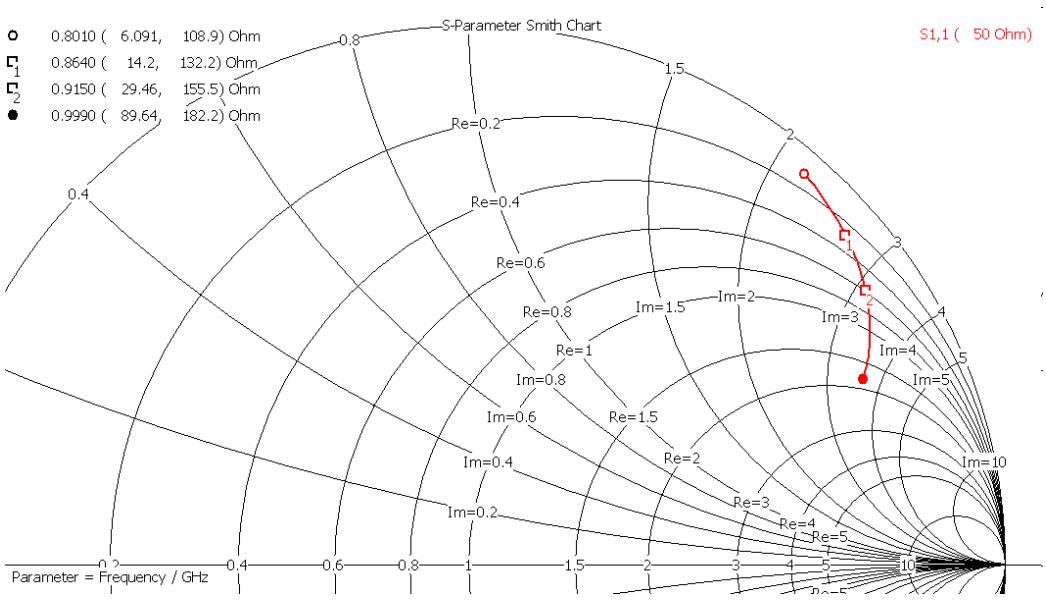


Fig 21. Smith Chart Position C : Simulated impedance of the PCB antenna for 4 different frequencies

Interpretation:

Fig 21 shows the impedances for difference frequencies. Target is to match the impedance of 20 – j140 (IC, 915 MHz). The simulations show, that the matching impedance is located between the impedance of 864 MHz (14,2 + 132,2 Ω) and 915 MHz (29,46 + j 155.5 Ω)

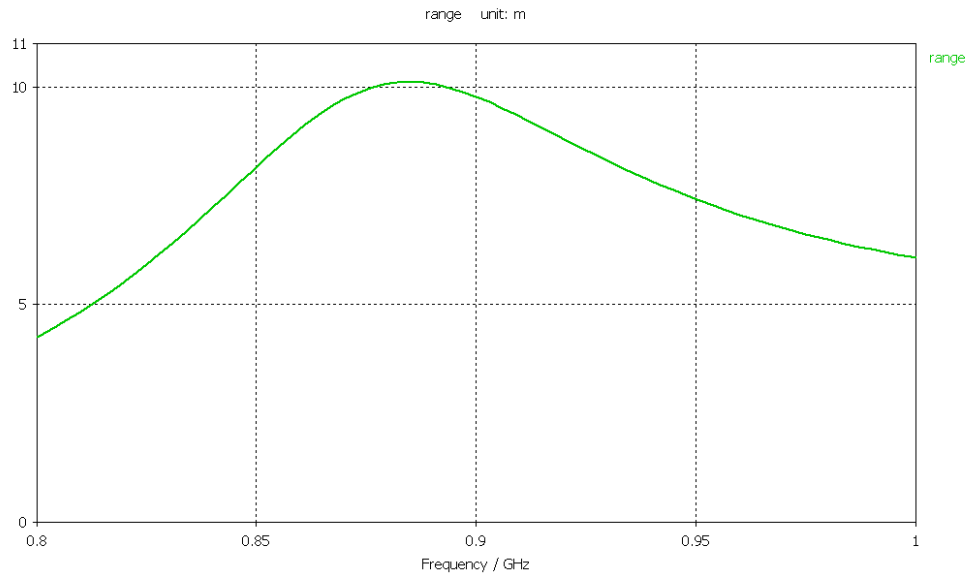


Fig 22. Simulated read range for slot position C

Fig 22 confirms the interpretation of the smith chart: The resonance point (maximum read range) is located at approximately 880 MHz, which is between the two impedances depicted in Fig 21 [864 MHz (14,2 + 132,2 Ω) and 915 MHz (29,46 + j 155.5 Ω)].

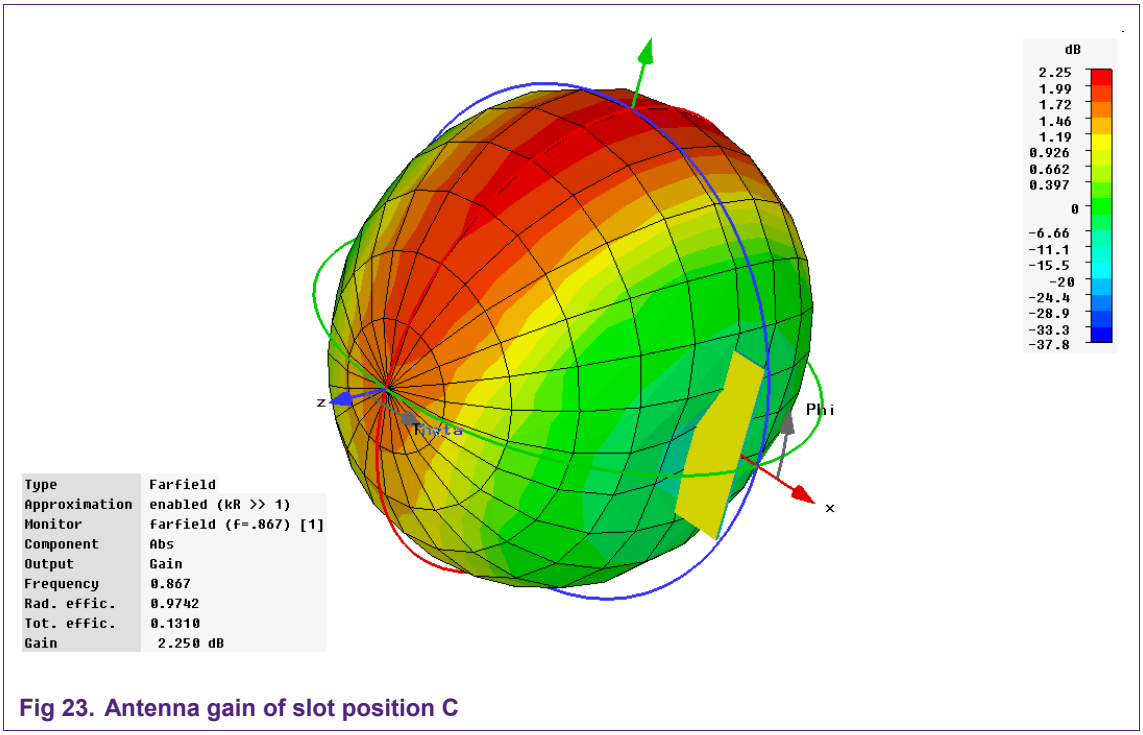


Fig 23. Antenna gain of slot position C

From the antenna gain pattern shown in Fig 23 we can see that the maximum gain has a positive value of 2,250 dB. Therefore, it has a better characteristic than the slot position B (Fig 19)

Interpretation: Both, position B and position C are symmetrically placed on the board. However, there is a performance difference of up to 5 meters (position C performs better). This is due to the face that the gain characteristic of the antenna changes, depending on the electrical length of the dipole, assuming that we simplify the characteristic to dipole properties. The gain is directly proportional to the length. The dipole length should be at least λ/2 in order to maximize the performance. Practically, these are approximately 10 cm. Thus, even though the matching is in both positions (B,C) good, the performance varies.

5.3.3 Position D

Position D shows just minor differences to position C

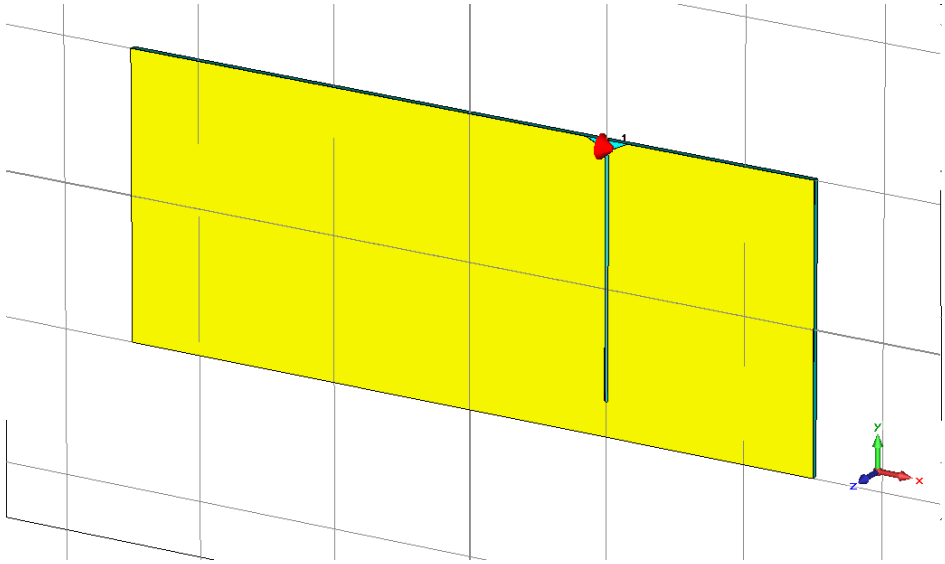


Fig 24. Slot positioning- Case D

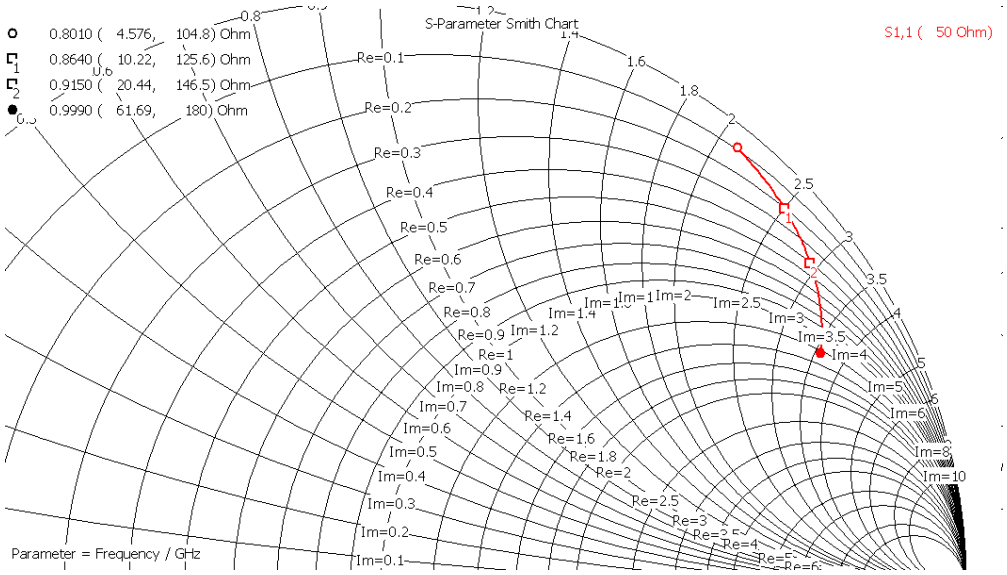


Fig 25. Smith Chart Position D: Simulated impedance of the PCB antenna for 4 different frequencies

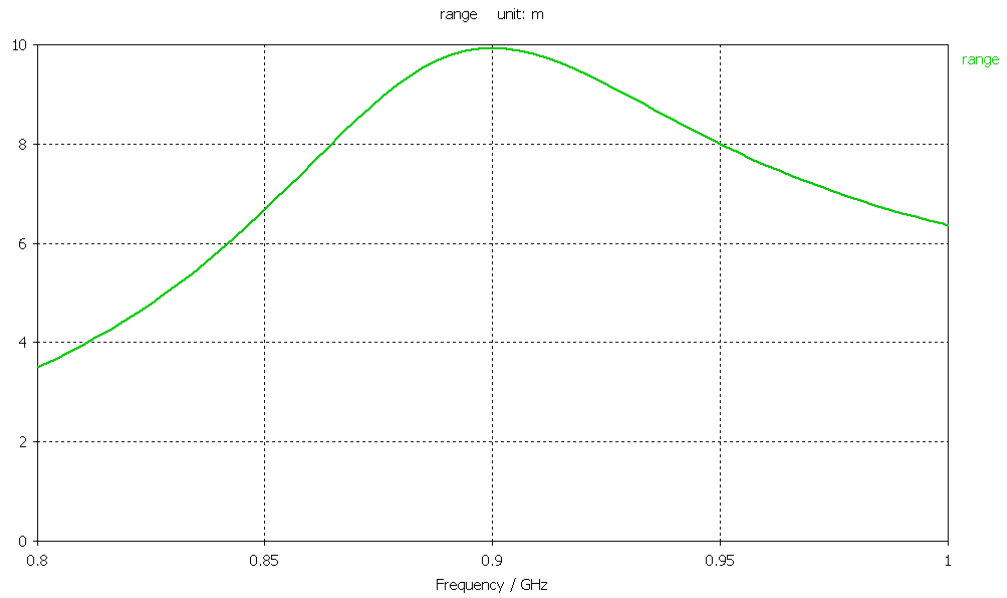


Fig 26. Simulated read range for slot position D

Compared to position C, the resonance frequency has shifted up to approximately 900 MHz.

5.3.4 Position E

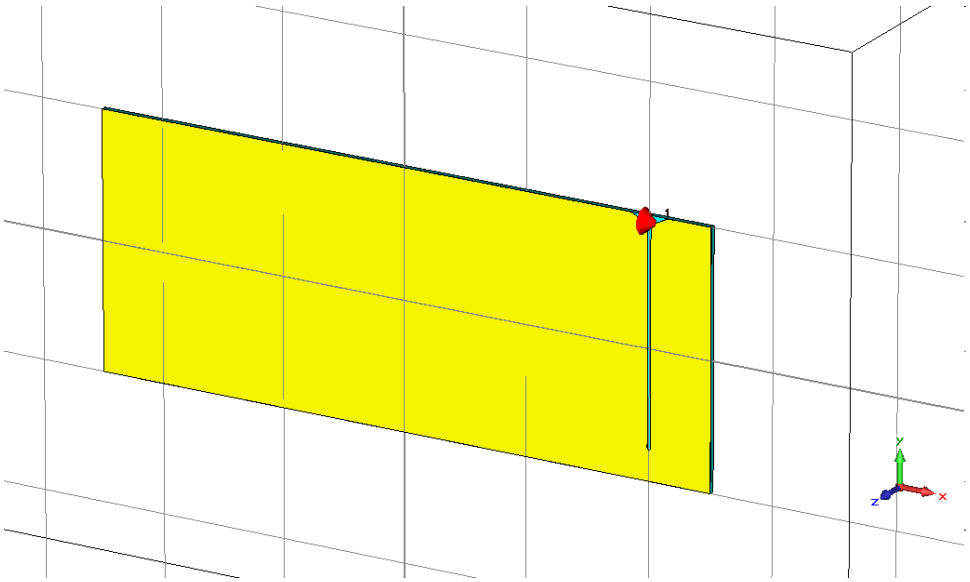


Fig 27. Slot positioning- Case E

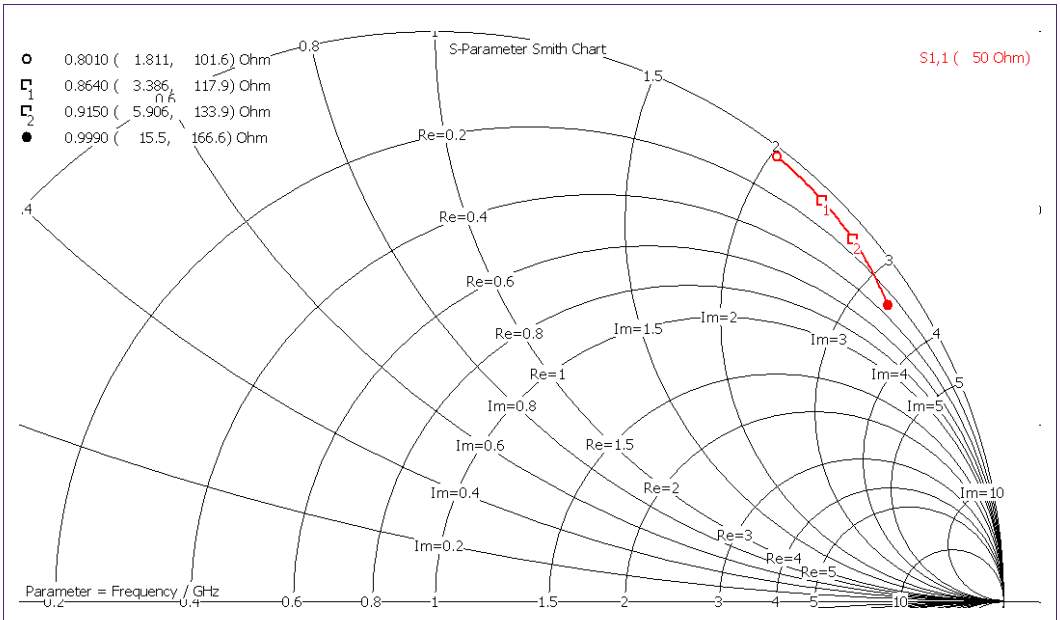


Fig 28. Smith Chart Position E: Simulated impedance of the PCB antenna for 4 different frequencies

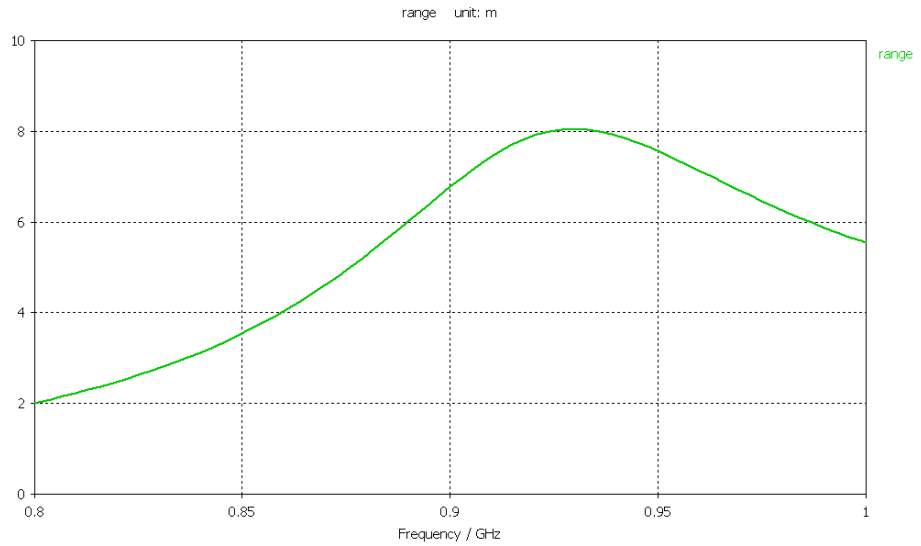


Fig 29. Simulated read range for slot position E

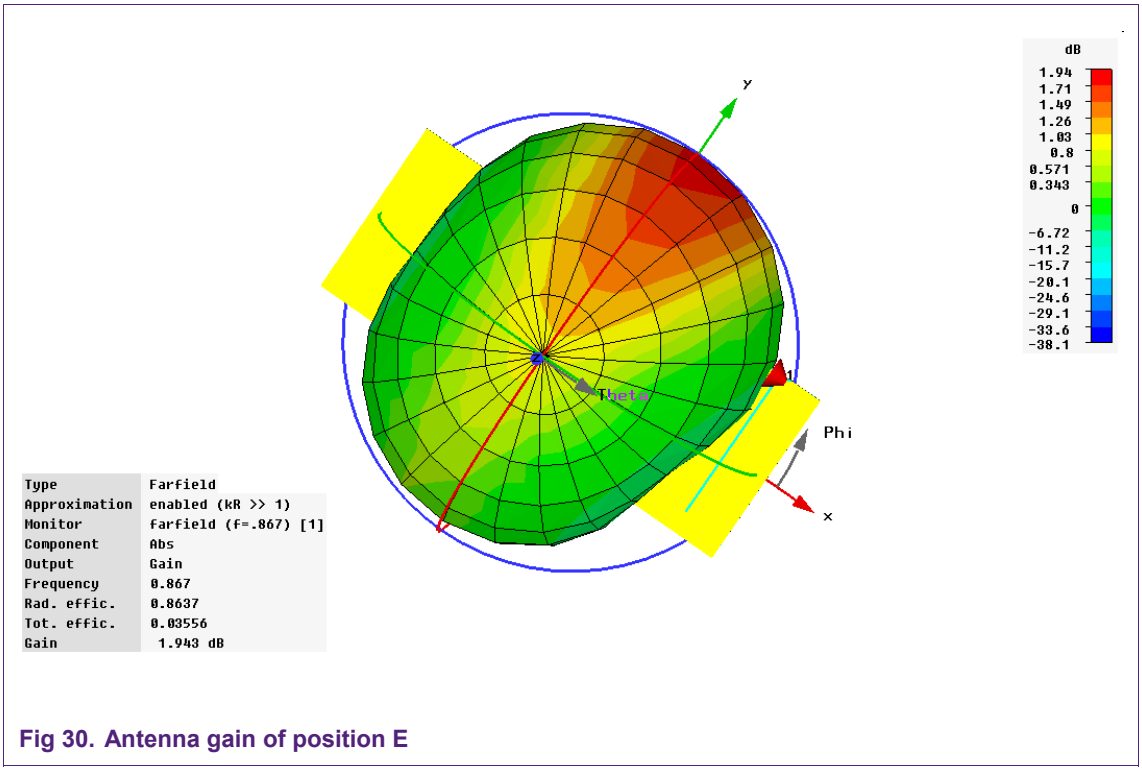


Fig 30. Antenna gain of position E

Position E already shows a significantly decreased performance. The resonance point is located very high at approximately 925 MHz with a maximum of 8 meters read range. The maximum gain is 1.9 dB.

5.3.5 Position F

The slot is placed at the very edge of the PCB, what makes the antenna geometry extremely asymmetric.

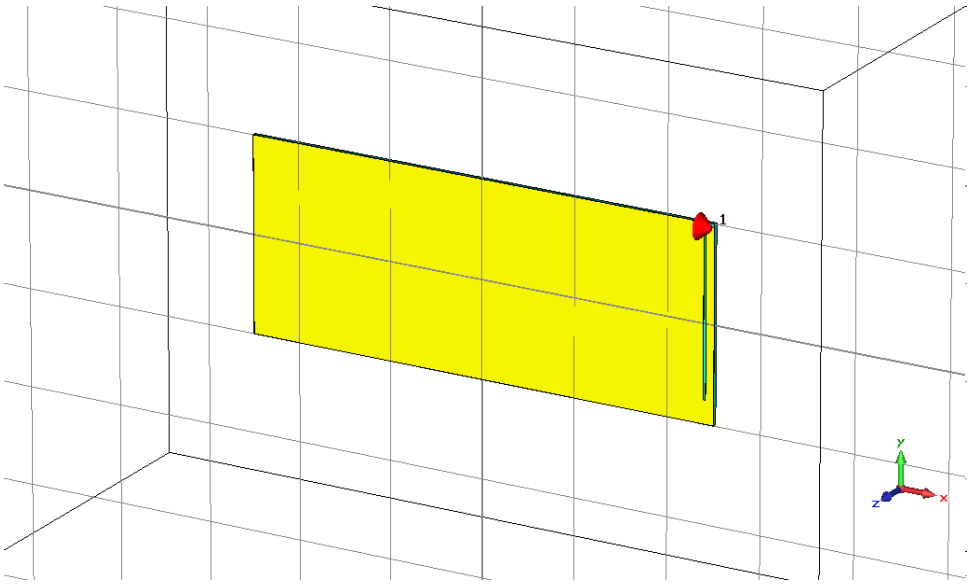


Fig 31. Slot positioning- Case F

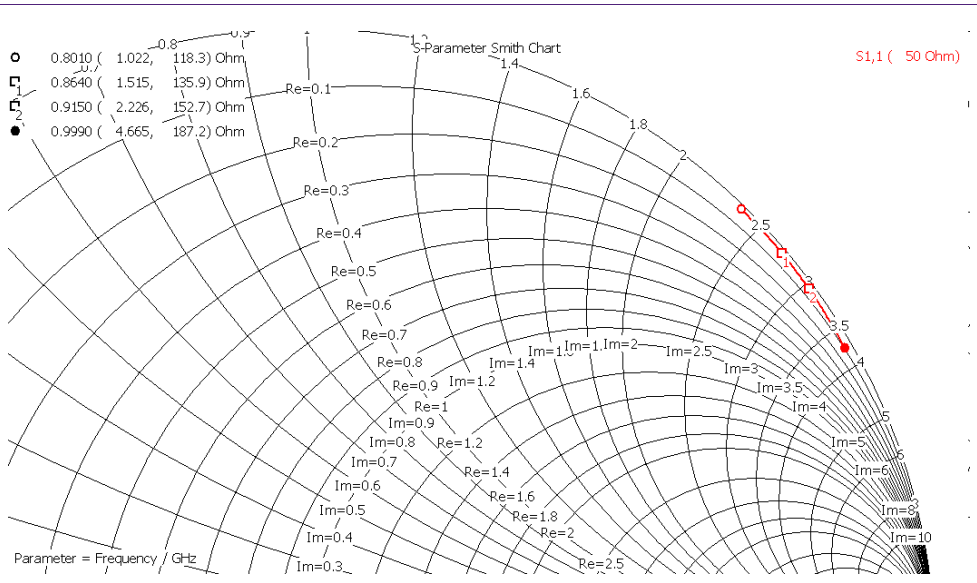


Fig 32. Smith Chart Position F: Simulated impedance of the PCB antenna for 4 different frequencies

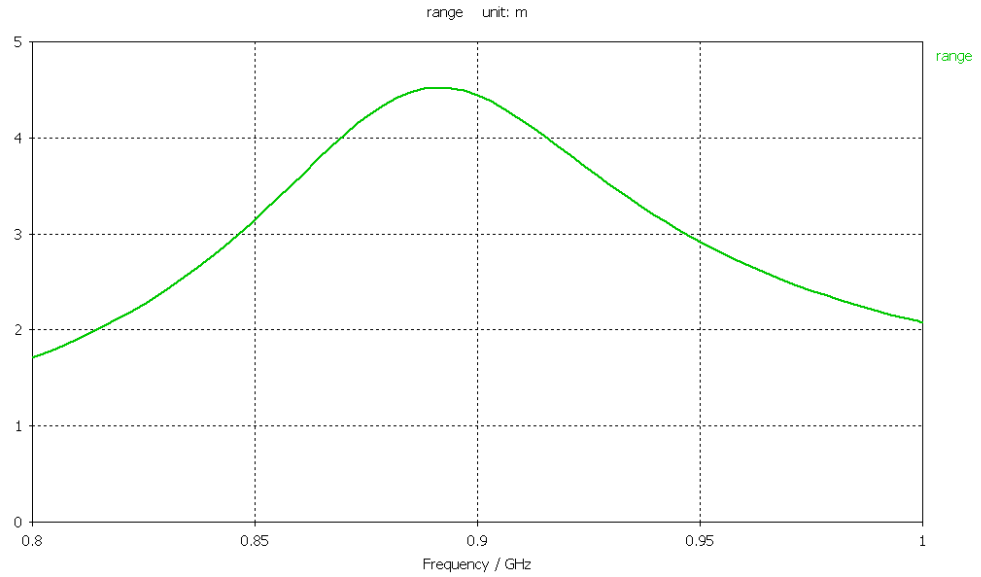


Fig 33. Simulated read range for slot position F

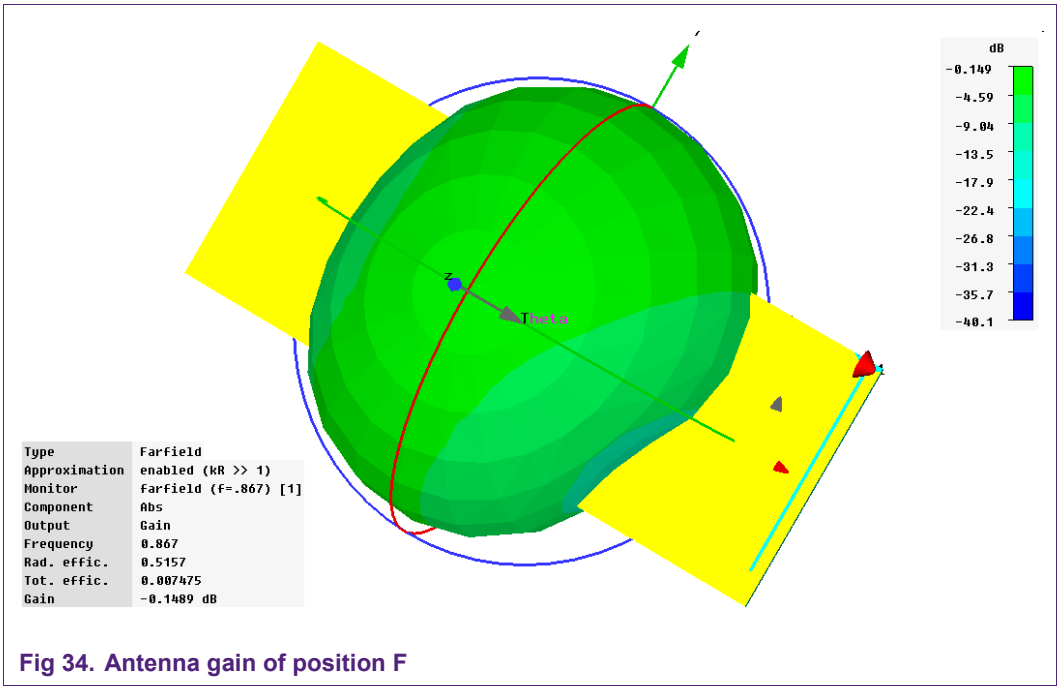


Fig 34. Antenna gain of position F

Interpretation of above Figures Fig 31- Fig 34: The maximum gain has a negative value of -0.14, the maximum read range has decreased to 4,5 meters.

6. Reference Designs

This chapter shows different real life examples, which are based on the background given in previous chapters. Since every PCB is different, the basic concept needs to be adapted to the respective boundary conditions.

It is a practical approach to RFID PCB tagging and shows two different concepts of PCB antennas, the slot antenna and the loop antenna concept, both based on UHF RFID technology.

It provides a guideline for implementing RFID onto a PCB board. The read range results are indications, and may change depending on components assembled on the board and reading environment

6.1 Reference Design - Slot antenna

Based on the simulation results from chapter 5.3 (up to 10 m read range at maximum) a symmetric slot position was chosen for the NXP PCB slot reference design. Two different slot lengths were manufactured, with the consequence that the resonance frequencies are slightly shifted. In this way, one design shows its peak performance in the European frequency range, and one under the FCC (USA) regulation.

Example case:

Layers	**1 (Single layer)**
PCB Dimension	**100 mm x 40 mm**
Slot	**2 different slot size (34.5 mm and 31.4 mm)**
Substrate	**FR4**
Substrate thickness	**1.5 mm**
Antenna material	**Copper**
Antenna material thickness	**35 µm**

Fig 35. Properties of slot antenna reference design

Fig 36. Layout of NXP PCB reference design

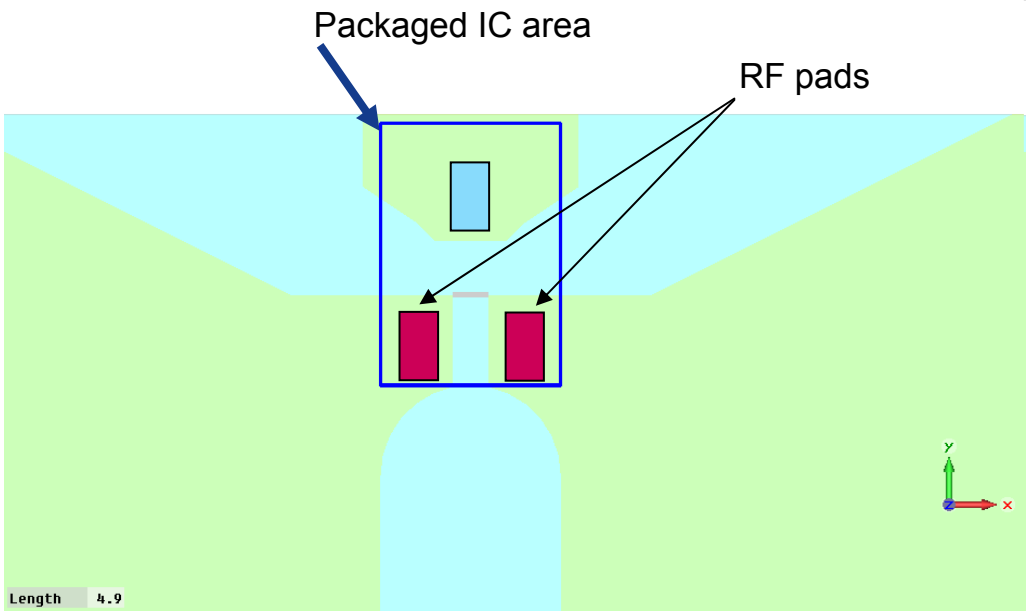


Fig 37. Attaching the SOT1122 package

Details of the SOT1122 package are included in the UCODE G2X functional specification.

6.1.1 Dimension

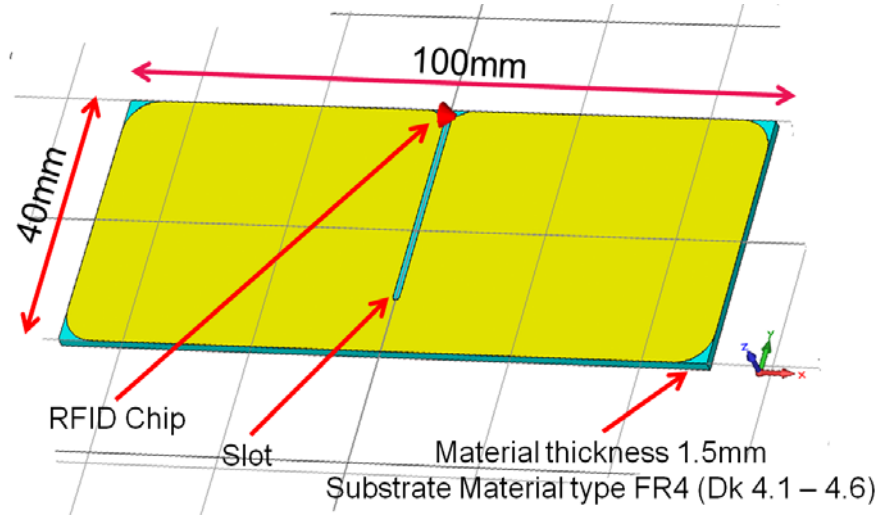


Fig 38. Dimensions of the slot antenna PCB

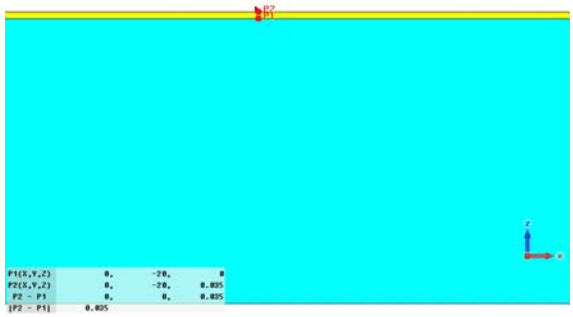


Fig 39. Copper layer thickness: 1.5 mm

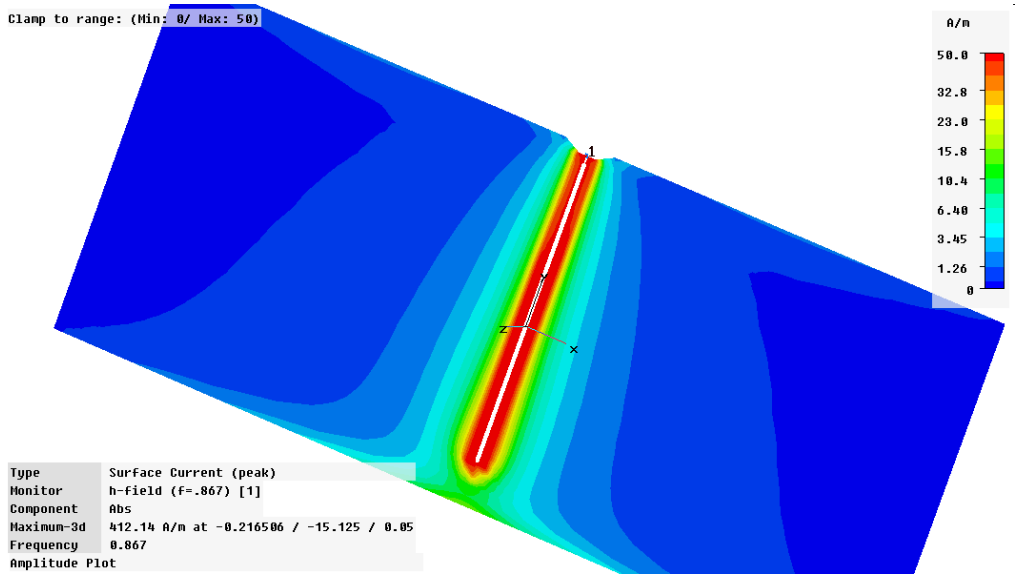


Fig 40. H-Field distribution

Above figure shows the distribution around a symmetrically placed slot. For a practical application, following should be taken into consideration:

The following steps should be consider before designing slot antenna on a PCB

1. **Antenna area requirement:** The size of the effective antenna area (copper layer) on a PCB should be at least 5 times the slot width (W). In other words, on each side of the slot there should be at least a metallization area of 2*W each.
2. **Width area clearance:** No vias and components should be placed in an area surrounding 2 mm of the slot antenna, due to the high density of the magnetic field strength.
3. **Slot dimension:** Changing the slot dimension and placement will decrease the optimum performance. The ideal slot dimensions will also depend on the substrate (thickness and material). It is not necessary to design slot antenna in one dimension. Slot antenna can be design by turning the angle of the antenna in various directions. The resulting performance is shown in the next chapter of this document.

6.1.2 Prototypes of the slot antenna: Two versions with different slot lengths

This Section gives the practical example of the calculation given in Chapter 5.

Practical example (2):

IC:

The IC is packaged into SOT1122.To match assembled IC with an equivalent series impedance of 18.6 - j171.2 Ohm at 915 MHz. If the package is assembled, parasitic capacitances are added (in parallel to the serial capacitance). Therefore, the resulting assembled and packaged IC impedance has approximately the value of:

Z_{IC} = 20-j155

PCB:

The real PCB does not consist of pure FR4 and is covered by an additional lamination layer. That leads us to following values:

Carrier material (substrate): ε_R = 4.9

In order to approximate the real case further, we modify equation 29(41) in the following way:

$$\varepsilon_{reff} = \frac{(\varepsilon_r + 1)}{2} + 1 \Longrightarrow \frac{(\varepsilon_r + 1)}{2} + 1{,}5$$

Substrate height h = 1.6 mm

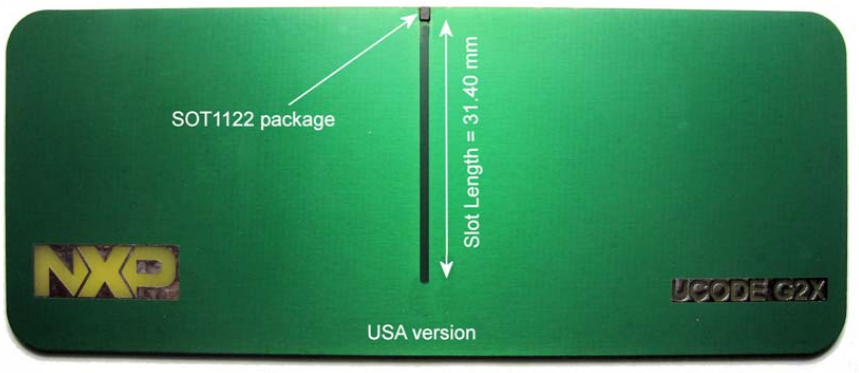
Slot line:

Definitions of the slot dimensions:

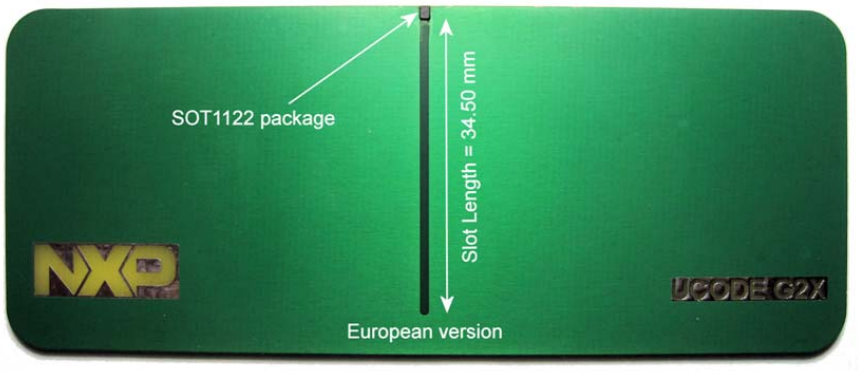
Width W = 1 mm

Length L_EU = 34,5 mm

Length L_US = 31,4 mm



Width W = 1 mm; Length of USA version = 31.40 mm



Width W = 1 mm; Length of European version = 34.50 mm

Fig 41. 2 versions of the reference designs (vary in slot length)

6.1.3 P_{min} measurements results

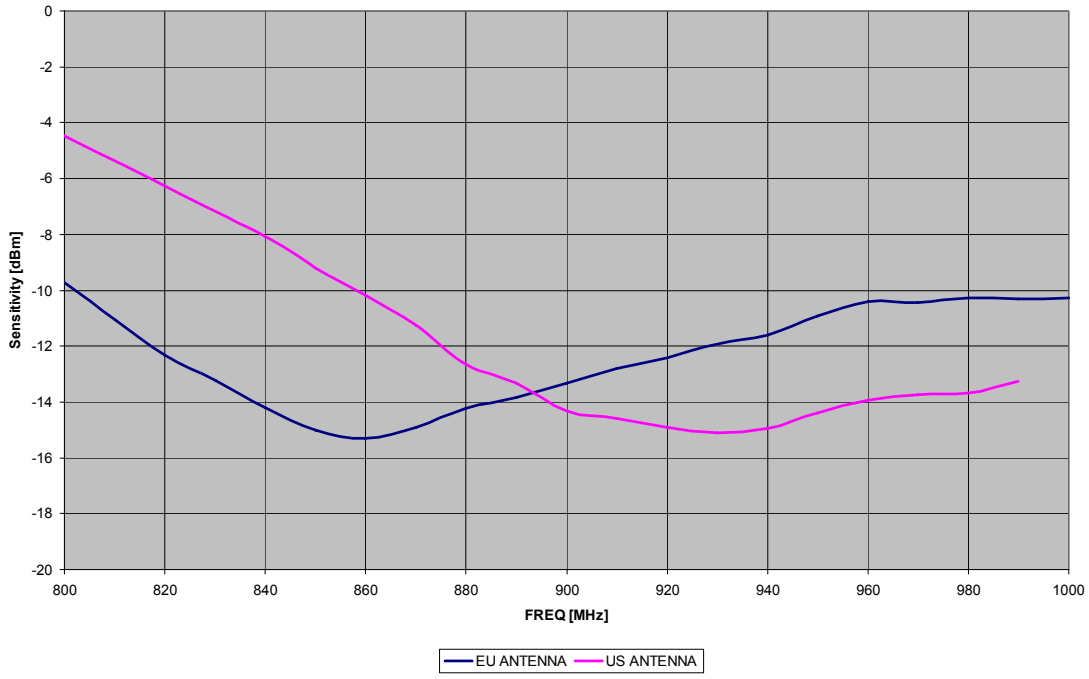


Fig 42. Measurement Results: Pmin-curve

6.1.4 Calculated read range

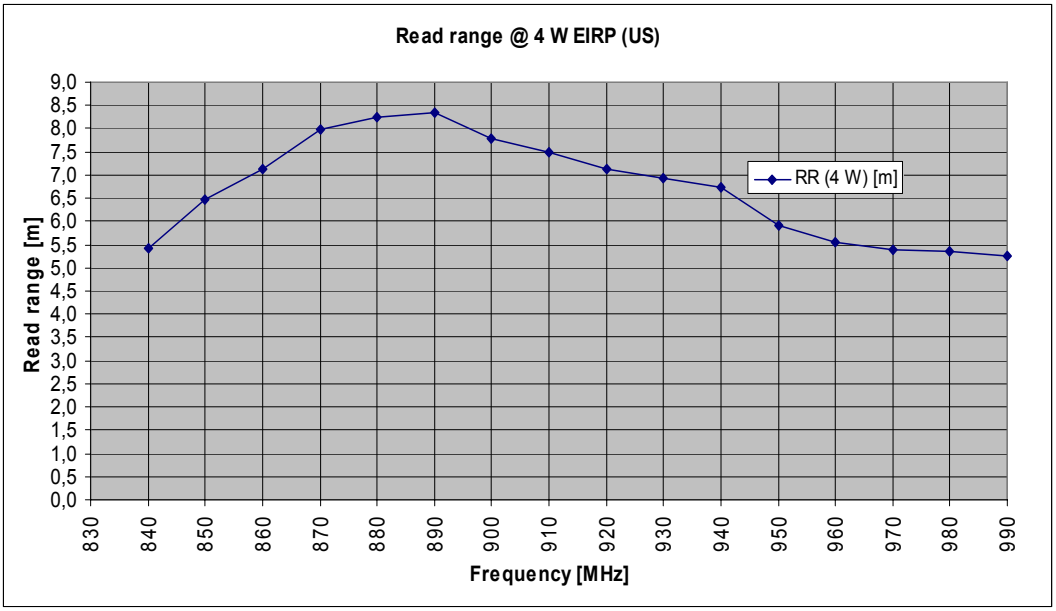


Fig 43. Calculated read range for the US tuned PCB (FCC regulation)

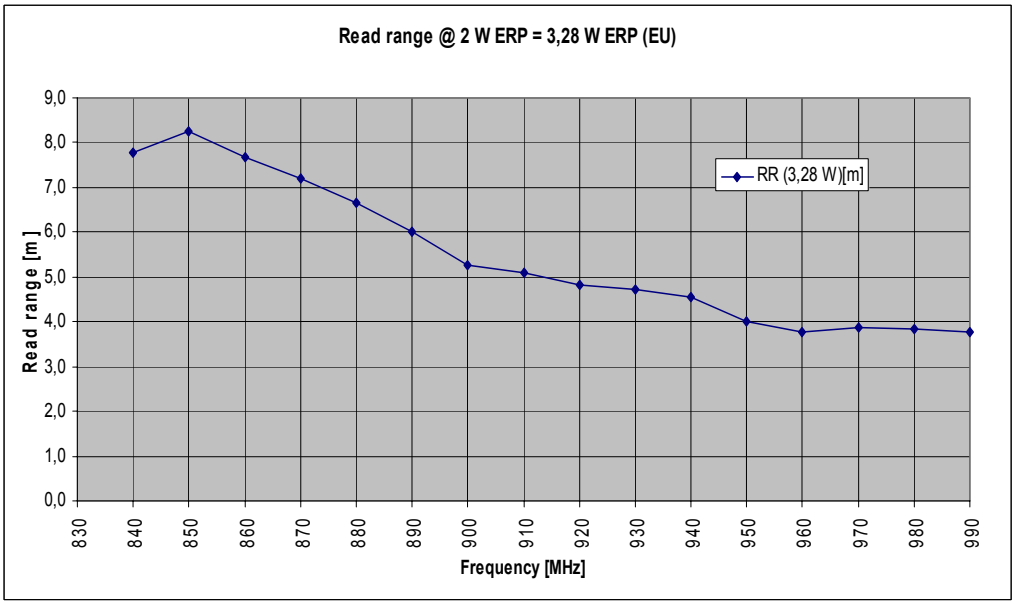


Fig 44. Calculated read range for the EU tuned PCB (ETSI regulation)

6.2 Reference Design: generic phone board

In this example of a phone PCB, a straight slot could not be realized due to design restrictions. The slot is slightly bigger than the straight sloth which is presented in Chapter 6.1. This is due to the reduced thickness of the substrate. The proportion between slot dimension and substrate thickness can be found in Chapter 5.

Antenna Description:

Table 1.

Label Type	Generic phone board reference antenna
IC Type	NXP UCODE G2X SOT1122

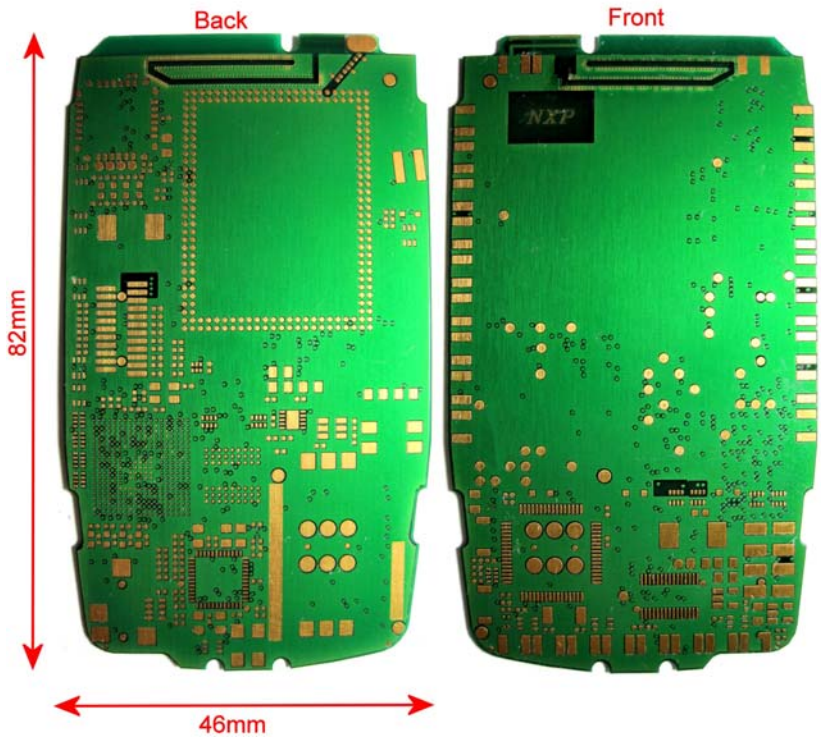
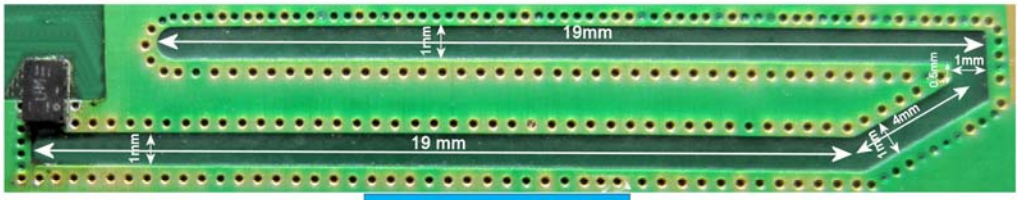


Fig 45. NXP generic phone board, front side and back side



Slot area		
Area 1	19 x 1 mm	19 mm²
Area 2	4 x 1 mm	4 mm²
Area 3	1 x 0.5 mm	0.5 mm²
Area 4	19 x 1 mm	19 mm²
	Total area	42.5 mm²

Fig 46. Slot area

Layers	**4**
PCB Dimension	**46 mm x 82 mm**
Substrate	**FR4**
Substrate thickness	**120 µm FR4 between copper layer 1 and 2** **200 µm FR4 between copper layer 2 and 3** **120 µm FR4 between copper layer 3 and 4**
Slot area	**42.5 mm²**
Antenna material	**Copper**
Antenna material thickness	**35 µm**

Fig 47. Properties generic phone board reference design.

6.2.1 Read range

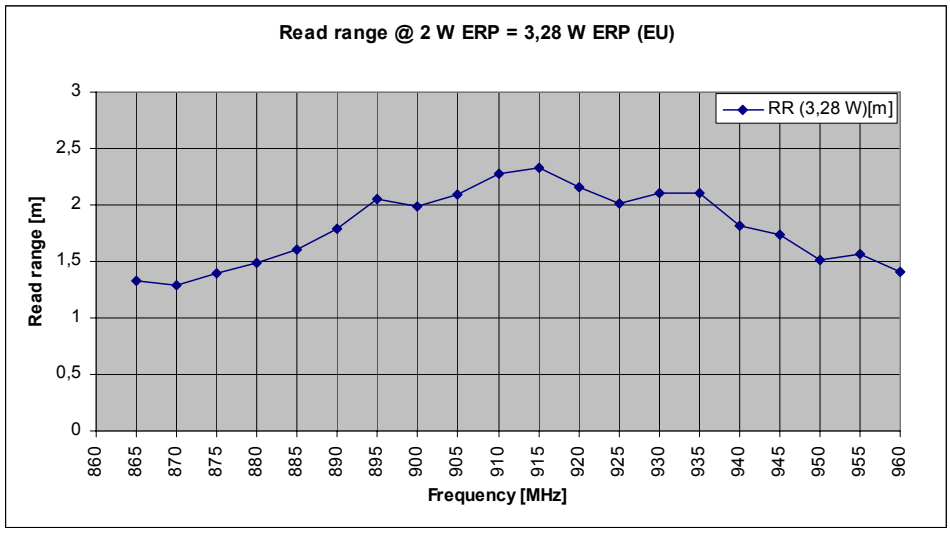


Fig 48. Calculated read range (ETSI regulation)

Fig 48 shows a read range of more than 2 meters for the USA frequency band, and more than 1 meter for the European frequency band. This is a performance drop compared to the slot shown in the first example, which shows a read range of up to 8 meters. This drop has two main reasons:

1) Asymmetrical placement: This reduces the gain of the antenna and therefore also the read range.

2) Bending of the slot: The target of this antenna was to fit the slot in an existing design, the drawback of the bending is the reduced read range due to increased losses.

6.3 Loop PCB

This example is based on following concept:

The IC is connected to a loop antenna. The final read range is depending on where this loop is implemented on the board. The area of the loop in this example is 5 mm x 5 mm, and it is implemented over 4 PCB layers.

Although the required space for the loop is very small compared to the slot antenna designs, there are still some boundary conditions, such as a certain clearance area or an additional antenna trace, which are required in order to guarantee a stable performance

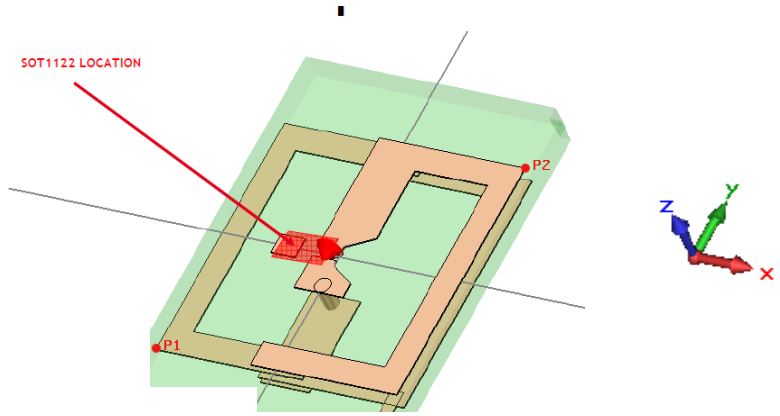


Fig 49. Structure of the PCB loop

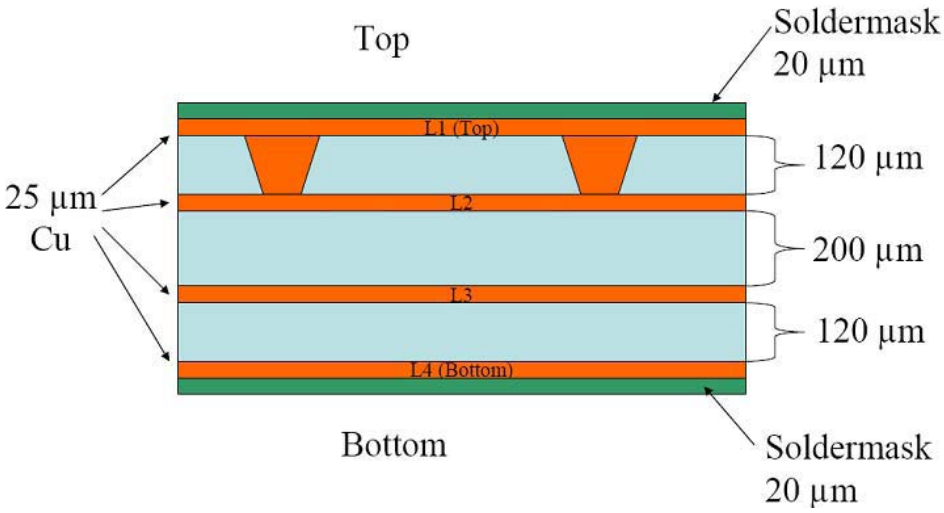


Fig 50. Layer structure of the 4 layer PCB board

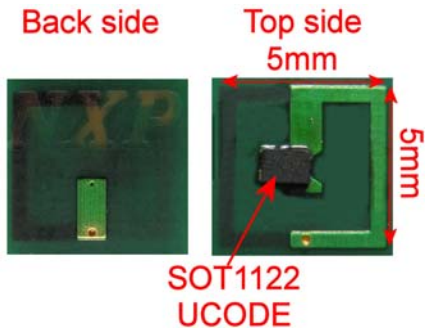


Fig 51. Picture of PCB loop samples

6.3.1 "Do´s and Don´ts" of using the loop concept on a PCB

The target of this section is to derive easy-to-use rules for implementing the loop on a PCB:

Two main aspects will have influence on the read range performance:

- ***Space:*** The loop should have a certain distance to the conductive area of the PCB (eg ground plane). Ideally the loop is very close to the conductive trace or area, but not touching it (below 1 mm). The distance can be up to 20 mm if the existing design requires it.
- ***Antenna:*** The loop needs a secondary antenna structure in order to achieve read ranges beyond a few mm. In the optimum case this is a "λ/2 antenna". This means a wire (or copper trace) of half of the wavelength. The used frequency depends on the local regulation. Table 2 shows the different wavelengths for the entire UHF RFID frequency band.

Table 2. Frequency to wavelength conversion (free space)

Frequency [MHz]	Wavelength (λ) [mm]	λ/2 [mm]
840	357,1	178,6
850	352,9	176,5
860	348,8	174,4
(EU) 870	**344,8**	**172,4**
880	340,9	170,5
890	337,1	168,5
900	333,3	166,7
910	329,7	164,8
(USA) 920	**326,1**	**163,0**
930	322,6	161,3
940	319,1	159,6
(Japan) 950	**315,8**	**157,9**
960	312,5	156,3

- ***Basic concept:***

Fig 52 shows the basic idea of how the loop can be implemented. The achieved read range in this case is 4.4 m. “L” corresponds to the half wavelength of approximately 172 mm. The main task of the loop is to match the impedance of the packaged IC, in case of the UCODE G2X in SOT1122 package this is 18.6 - j171.2 Ω.

The IC has a capacitive impedance, in order to match it an antenna should be inductive. Since the impedance of a simple dipole is not inductive, it needs an additional matching element such as this loop.

Simply expressed, the loop matches the impedance, while a second antenna trace adds the necessary gain to the antenna in order to achieve read ranges of several meters.

Of course, there is not always enough space for implementing a “λ/2 antenna”.

What is the influence on the read range if the antenna length drops to λ/4 ?

Cutting the antenna length will displace the resonance frequency from 868 MHz (EU frequency) to a much higher frequency. Having a λ/4 antenna, the read range will drop to < 0.5 m

- ***General note: Read range results are only indications and my vary, depending on reader antenna characteristics and environment***

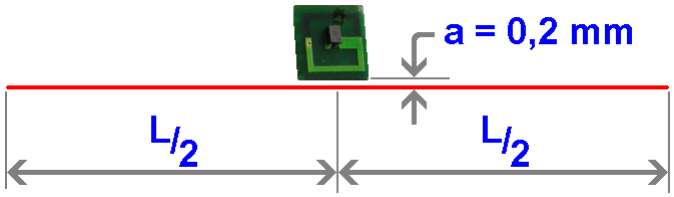


Fig 52. Basic concept of using a loop antenna with a wire of L= λ/2 as an antenna, 4.4 m read range

- ***How can this be translated to a PCB?***

6.3.2 "Do":

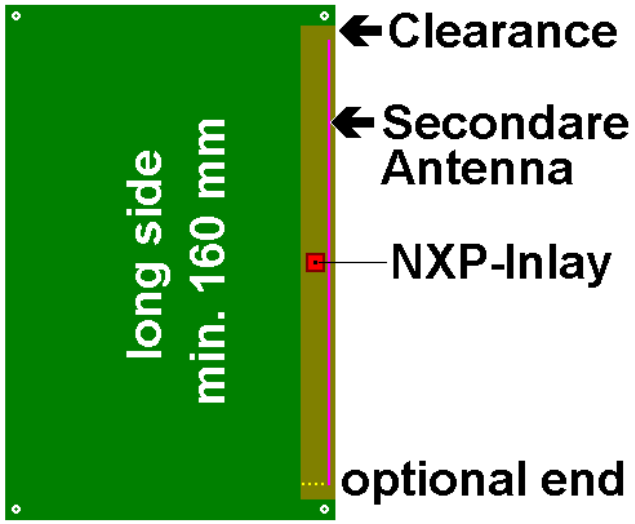


Fig 53. The ideal case – loop plus λ/2 dipole

The width of the clearance (non-conductive area, such as FR4 material) should be at least 5 mm, as the loop has a width of 5 mm, and some additional spacing between ground plane and loop is required.

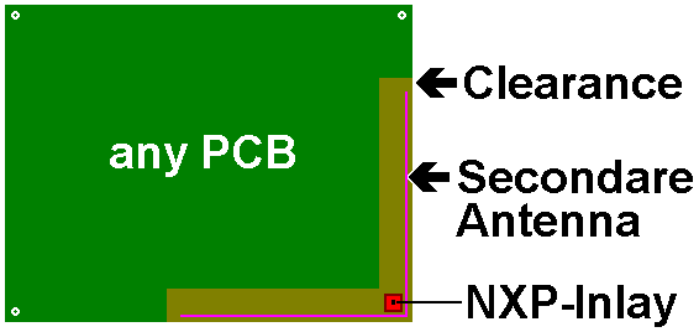


Fig 54. The loop can also be placed on the edge

Fig 54 shows the placement on the edge. Every arm has ideally the length of λ/2

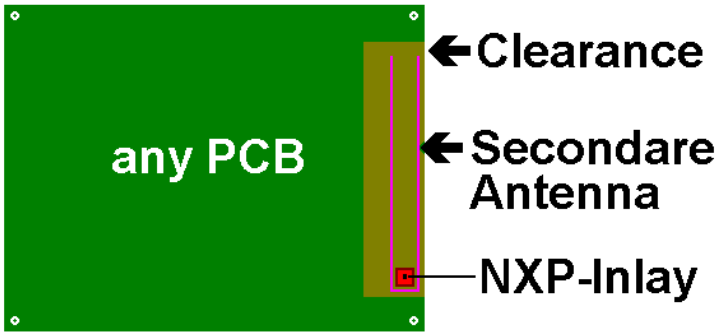


Fig 55. A turned dipole will require less length

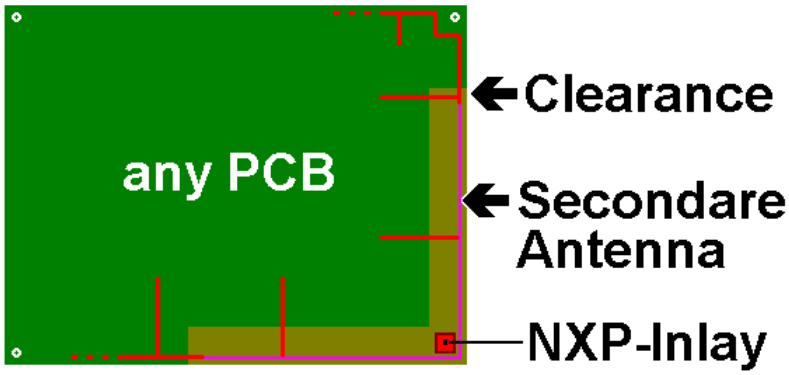


Fig 56. Secondary antenna structure consists of existing PCB traces

6.3.3 Don´t

- Place the loop surrounded by conductive material:

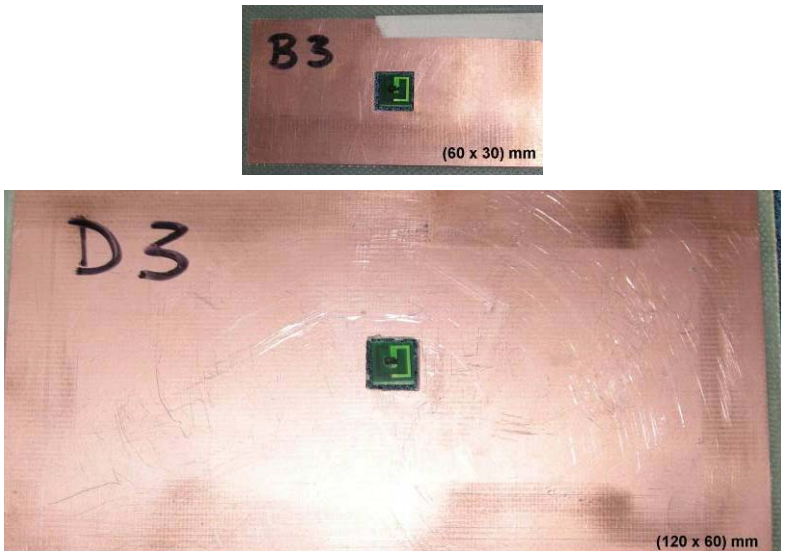


Fig 57. Don`t: loop surrounded by copper

- Place the loop between two conductive traces. In this way the induced currents will cancel each other.

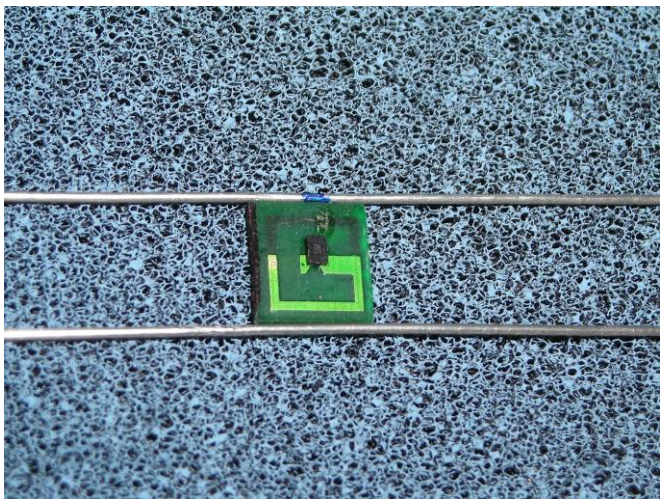


Fig 58. Don`t : between two wires (traces)

6.3.4 Influence of placement to the read range

This section contains the change of the read range when the loop is moved out of the center near the edge of the copper plane.

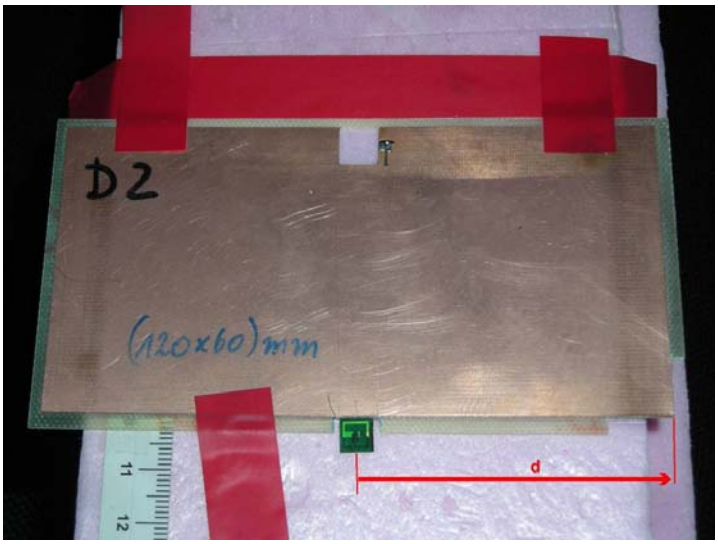


Fig 59. Moving the loop, starting from the middle , to the edge of the copper plane

Results:

d = 0 (loop centered) → readrange = ~1,2 m

d=12 mm → readrange = ~1.1 m

d=24 mm → readrange = ~ 1m

d= 36 mm → readrange < 0.5 m

Loop placed on the edge: no read

Since the loop was not readable when it was placed on the edge of the PCB, it was tried to place the loop into a cut edge:

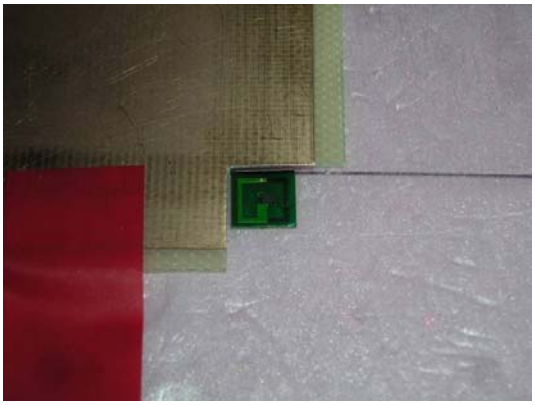


Fig 60. Cutting edge: read range < 0,5 m

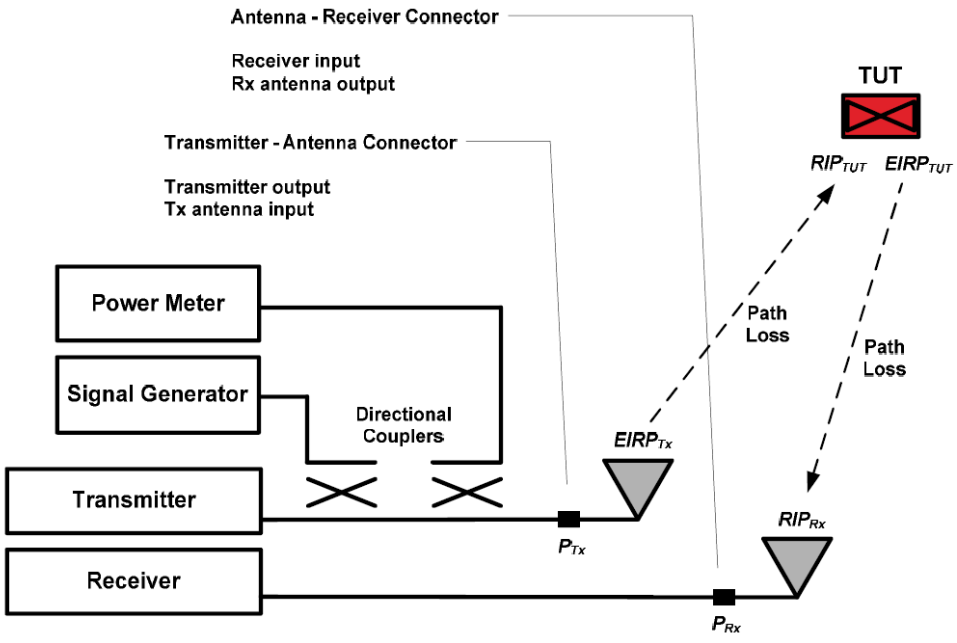
7. Measurement Method

The measurements were conducted with label prototypes. Therefore possible performance tolerances have to be taken into account.

7.1 P_{min} measurement

The minimum power measurements are carried out in an anechoic chamber, according to the measurement setup described in the EPC global document “Tag Performance Parameters and Test Methods Version 1.1.1”.

The information gained from this measurement method is the minimal required power level at the label for powering the IC. This minimal power (P_{min}) is measured for a defined frequency range from 840 MHz to 990 MHz. Fig 61 shows the P_{min} measurement results of all assembled antennas.



source: EPC global document “Tag Performance Parameters and Test Methods Version 1.1.1

Fig 61. Block diagram of the measurement set up

8. Conclusions

This application note provided initially the necessary theoretical background for UHF RFID antennas, and as a second step also for the implementation of an UHF RFID antenna on the PCB. As the available area on a PCB is extremely limited, a slot antenna design was chosen as a first approach, as it minimizes design effort, is variable in terms of placement of the slot on the PCB, and it uses a minimum of PCB space.

By means of 3D simulation tools, the optimum placement and dimension of the slot antenna was evaluated.

In order to verify the simulation results, prototypes were manufactured. The performance of the prototypes was measured with a standardized measurement setup in an anechoic chamber.

The second part of this document described available reference designs. Two of them are based on the slot concept, and a third one is based on a loop concept. Each of them has advantages and disadvantages, the choice depends on the available space, number of layers, read range requirements etc.

The NXP reference antenna designs for PCBs shall give a starting point for customers for designing an RFID antenna for PCBs.

9. References

[1] Microstriplines and Slotlines, K.C. Gupta

[2] Tag Performance Parameters and Test Methods vs 1.1.2, EPC global

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11. Contents

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Date of release: 21 January 2010
Document identifier: AN_1715